University of Sussex

Doctoral Thesis

The Geonium Chip

engineering a scalable planar Penning trap

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A thesis submitted in fulfilment of the requirements for the degree of Doctor of Philosophy

in the

Geonium Group
School of Mathematical and Physical Sciences

University of Sussex

February 2017

Declaration of Authorship

I, Jonathan PINDER, declare that this thesis titled, 'The Geonium Chip - *engineering a scalable planar Penning trap*' and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

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Abstract

Atomic Molecular and Optical Physics
School of Mathematical and Physical Sciences

Doctor of Philosophy

The Geonium Chip - *engineering a scalable planar Penning trap*

by Jonathan PINDER

In this thesis is presented the realisation of 'The Geonium Chip', a novel planar Penning trap. The chip is designed with the goal of building a truly scalable planar Penning trap, while retaining the accuracy of 3D traps. Manufactured with conventional metal-on-silicon microfabrication techniques, the chip takes the 5 electrodes of the compensated cylindrical trap and projects them onto a ground-plane surface, thus forming the basis for its layout by reducing the electrode shape to an array of flat rectangular surfaces. In this thesis I describe the conception, design and construction of a full cryogenic set-up, including the magnetics, for trapping and observing a single electron in the Geonium Chip Penning trap. The cyclotron mode of the trapped electron lies in the microwave regime, and thus the Geonium Chip has the potential to become a powerful building block for quantum microwave circuits, with coherent coupling to the cyclotron degree of freedom. This will also allow non-destructive measurement and interaction with the spin state of the electron. The development of the experimental process is detailed from scratch including the design, fabrication, and testing of the Geonium Chip, as well as the design, fabrication and testing of the experimental apparatus. The original solutions and space saving designs developed as part of the construction process are detailed, such as the custom on-chip cryogenic vacuum chamber, planar magnetic field source, and the LED-based electron loading system. The vacuum chamber and control systems are also described, and the in-house manufacturing capabilities of the Geonium group are detailed at length, with an emphasis on rapid prototyping high-accuracy components suitable for experimental use. The apparatus built within this PhD is within a few weeks of performing the first loading of electrons into the chip trap.

Acknowledgements

I would like to thank Dr. José Verdú-Galiana, for the continuous guidance offered throughout the course of this PhD, and without whom, none of this work would be possible. Thanks to April, John and Frances of the Geonium Chip group, whose help greatly accelerated the project. To Prof. Winfried Hensinger and Dr. Matthias Keller for kindly lending equipment, apparatus and software, and for providing numerous insights and expertise, aiding the progression of the project. To Dr. Bjoern Lekitsch for invaluable advice on microfabrication techniques, and Anton Grounds for helping with microwave analysis, low-temperature measurement techniques and pressurised gas handling. Thanks to Alex Burns, for supplying chemical consumables and providing high pressure gas fittings. I would also like to thank Dr. Ian Hepburn for providing a remedy for our cryocooler troubles, and for fruitful discussions about cryogenic techniques. Finally, to Richard Chambers, for helping to solve the administration issues encountered throughout the PhD process.

I would like to acknowledge *SEPnet* as the main source funding, and Colin Hayhurst and Seb Oliver for support through RDF funding. Thanks also to *American Superconductor* and to *Bruker Inc.* for their kind donations of specialised high-temperature superconducting tape.

In addition to work performed by the author, data has also been included where the majority of results have been obtained by other members in the Geonium Chip group, in order to better illustrate the points discussed in the text:

- **Section 2.2** The Geonium Chip mathematical model and 'Mathematica' simulation results presented throughout chapter 2 were written and obtained by group supervisor *Dr. José Verdú-Galiana.*
- **Table 3.4** The values presented in the table were obtained by PhD candidate *April Cridland.*
- **Figure 6.11** The graph presented was measured and plotted by PhD candidate *John Lacy.*

Contents

List of Figures

List of Tables

Abbreviations

2DEG	**2** - **D**imensional **E**lectron **G**as
ADR	**A**diabatic **D**emagnetization **R**efrigerator
CNC	**C**omputer **N**umerical **C**ontrol
CPW	**C**o **P**lanar **W**aveguide
DUT	**D**evice **U**nder **T**est
EBIT	**E**lectron **B**eam **I**on **T**rap
FEM	**F**inite **E**lement **M**ethod
FFT	**F**ast **F**ourier **T**ransform
FTICR	**F**ourier **T**ransform **I**on **C**yclotron **R**esonance
HTS	**H**igh **T**emperature **S**uperconductor
LN_2	**L**iquid **N**itrogen$_{(2)}$
MW	**M**icro**W**ave
OD	**O**uter **D**iameter
OFHC	**O**xygen **F**ree **H**igh **C**onductivity (Copper)
PT	**P**ulse **T**ube
UV	**U**ltra **V**iolet

Chapter 1

Introduction

1.1 Introduction

'You know, it would be sufficient to really understand the electron.'

Albert Einstein [21]

The idea behind the *'Geonium Chip'* stems from a wealth of previous inquiry into the field of charged particle entrapment, single electron trapping and observation. Since Penning's discovery of flight-time manipulation using electric and magnetic fields in 1936 [22], the area of electron confinement has progressed greatly. The concept was explored by Nobel laureate H.G. Dehmelt, who shared the Nobel prize in 1989 with Wolfgang Paul *'for the development of the ion trap technique'*. Dehmelt's group performed the first short-term magnetron trapping of electron clouds in the late 1950s, and single-electron trapping was achieved by Dehmelt's group in 1973 [23]. It was also Dehmelt who first coined the term *'Geonium'* [24], as a cloud of electrons confined in static fields can be likened to a multi-electron atom, with the nucleus supplanted for the confining apparatus. Since this essentially tethers the electrons to the earth to form a pseudo-elemental system, the name was formed by appending the common chemical element suffix '-ium' onto the Greek prefix for 'earth', to form Geonium. The *'Geonium Chip'* is so named in honour of this.

At the time of writing, there are numerous Penning trap research groups globally, across the USA, Europe, and Asia performing a wide range of experiments from mass-spectrometry [25, 26], measurements of the g-factor for the proton [27, 28] and electron [29], anti-matter experiments [30–32] and close study of a wide range of highly charged particles [33] to an ever increasingly precise degree. The 'Geonium Chip' aims to provide all the functionality and measurement accuracy achieved by existing Penning groups, but with a novel new planar electrode layout, and pioneering magnetic field source which come together in a compact system, designed to be mobile and also offer great reductions in size, weight, and cost.

1.1.1 Motivations and Inspirations

The project is driven with three primary goals in mind, branching off from the uses mentioned above. Planar Penning traps were first envisioned as building blocks for quantum computation, but the Geonium Chip is not designed with this primarily in mind, though future generations could still explore this area. Instead the Geonium Chip group seeks to exploit its compact form factor to create a portable Penning trap system with a planar magnetic field source, and the benefits that this would bring to systems in the following interest areas:

- **Mass Spectrometry** Mass spectrometry is a two-billion dollar industry globally, with interest in pharmaceuticals and chemical processing driving growth in the sector worldwide [1]. Currently, if highly accurate measurements are required it is necessary to send samples off to a spectrometry facility for analysis, a time consuming process. One of the goals Geonium Chip is to have a fully portable system, insensitive to vibration and external factors, allowing on-site analysis. A summary of cost vs resolution can be seen in figure 1.1, it shows that initial estimates of the expected resolution performance place the Geonium Chip in a region of the market not currently occupied by existing systems. Whilst the current incarnation of the Geonium Chip is set up to trap only electrons, the chip itself can trap any charged particle. Techniques for loading atomic and molecular ions into Penning traps and FTICR spectrometers are very well documented and routinely used, and so it would be possible to adapt the set up to accept ionized samples.

FIGURE 1.1: A graphic showing where the Geonium Chip as a mass spectrometer is predicted to fit into the mass-spec market, in terms of price and accuracy. When functioning, the Geonium Chip is predicted to give very good resolution for the price [1].

- **Broadband Single Microwave Photon Detection** High sensitivity in the Microwave frequency regime is required in fields such as brain research, terahertz wave security systems, and background radiation astronomy, yet there is currently no single microwave photon device on the market as of writing [34]. A single photon detector would allow systems to go to the absolute limit of sensitivity. The earliest known single photon detections in the MW range were observed in Penning traps [2]. Results from this experiment are shown in figure 1.2. By cooling the cyclotron motion down to the ground state, and applying a magnetic 'bottle' (a curvature in the B magnetic field) to the Penning trap, the energy of the cyclotron mode becomes linked to the axial frequency via the "*continuous Stern-Gerlach effect*". With a sufficiently accurate system, the absorption or emission of photons with frequency ω_+ produces a discrete, measurable, frequency shift in ω_z.

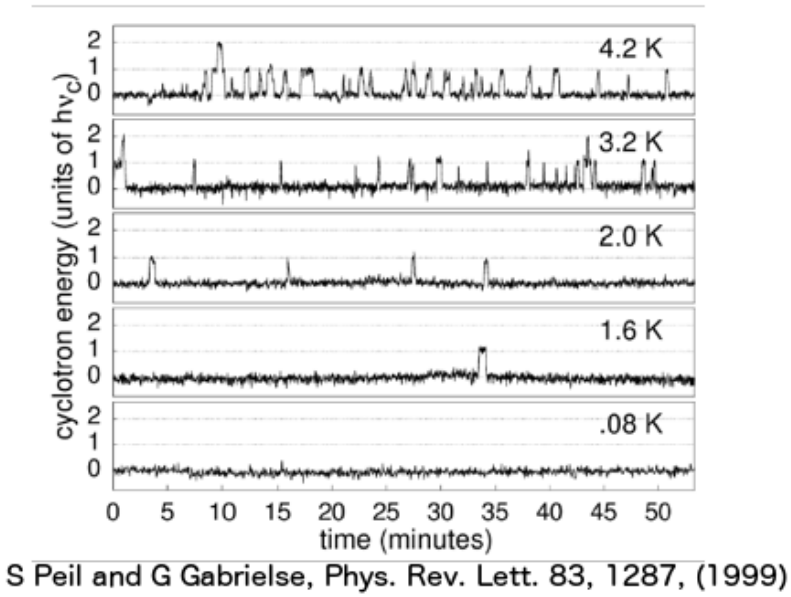
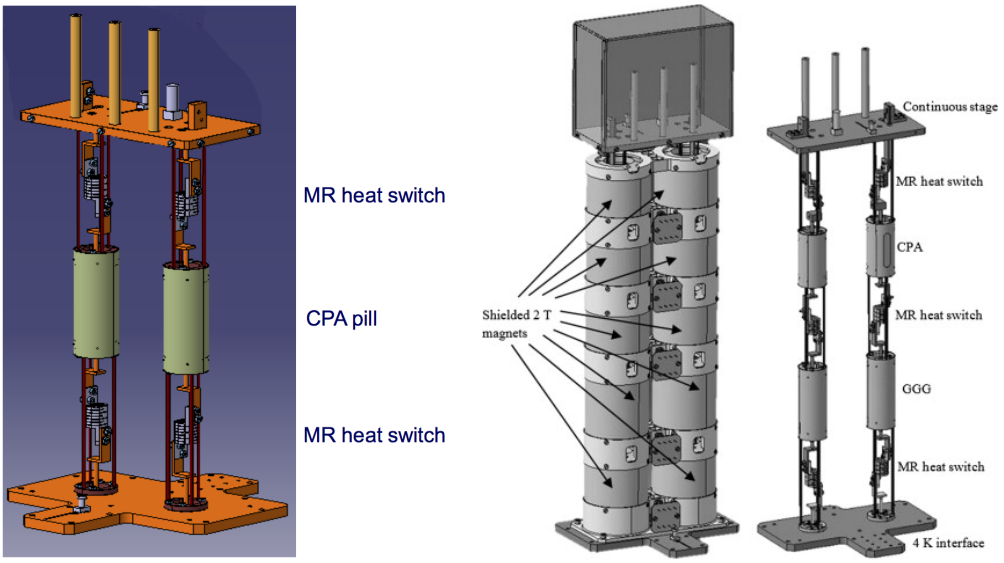


FIGURE 1.2: A demonstration of single microwave photon detection by the group of G. Gabrielse (1999)[2].

Although many groups are working towards single MW photon detectors, competing systems are largely based upon two-level systems, which although capable of single photon detection, are limited to just one photon measurement at a time. In a Penning trap, the cyclotron degree of freedom acts as a harmonic oscillator, and thus has any number of discrete energy levels separated by the photon energy $\hbar\omega$, as seen in figure 1.2. The Geonium group aim to make a compact system which includes the magnetic field source [15, 35]. In order to reach the cyclotron ground state, temperatures lower than the current system can achieve are required, and as such the Geonium group are in talks with MSSL in order to obtain an Adiabatic Demagnetisation Refrigerator device (ADR), capable of reaching the millikelvin range without moving parts, refrigerants, while having a compact form factor [3]. An example sketch is shown in figure 1.3



(a) (b)

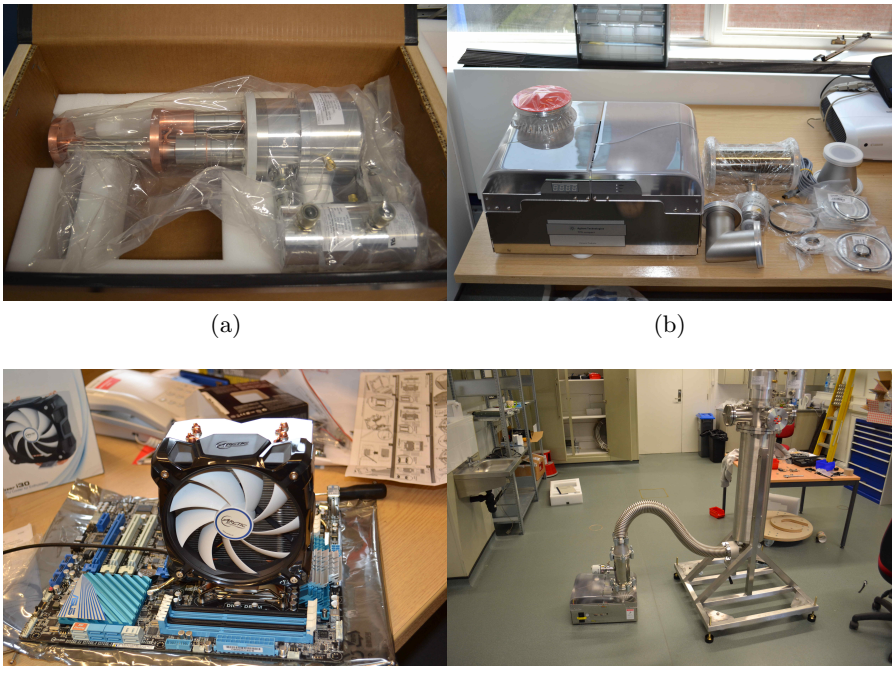
FIGURE 1.3: 1.3(a) shows an example of a single adiabatic demagnetization refrigerator (magnets not shown), which will reach a temperature of 250mK with a bath of 4K [3]. This compact device is just $120 \times 56 \times 250$mm, and weighs approximately 5kg. The 'MR switch' is magneto-resistive heat switch made of single-crystal tungsten, and is used to control the flow of heat between the Chromium-Potassium-Alum (CPA) 'pill'. The devices can be combined as shown in figure 1.3(b) to achieve better cooling over a wider temperature gradient by using different 'pill' compositions, in this case CPA and GGG (Gadolinium-Gallium-Garnet) [3, 4].

- **Improvements on Fundamental Measurements** The Geonium Chip has been designed to equal the performance of current 3D cylindrical traps, but there is an opportunity to build a system with improved resolution when compared to current experiments [6, 36–38] by working to reduce magnetic field instabilities. In the future generations of the Geonium Chip, the magnetic field will be incorporated into the substrate of the chip [15], and run in persistent mode. This should provide excellent magnetic field stability by eliminating physical vibrations and electrical noise - one of the main sources of error in high precision measurements - and allow improvements of fundamental measurements. As the Geonium Chip is designed to be primarily an electron trap, the first area of focus could be the measurement of the electron mass [24, 39].

Owing to the compact form factor of the Geonium Chip, it is not infeasible that a single cryogenic system could house multiple experiments simultaneously!

1.1.2 The Beginning of a New Experimental Group at Sussex

This thesis details the beginning of a new laboratory at *Sussex University*. Starting from an empty room, all equipment, tools, storage, plumbing, computers, and even the chairs and tables, were all installed from new as part of this project. For this reason, the thesis includes more basic technical information - vacuum pumps, temperature sensors etc. - than is perhaps common for a more usual experimental thesis, simply due to the amount of time dedicated to assembling the necessary parts. It should also be noted that the pace of work was limited by the fact that for much of the time covered in this work, the author was the sole member of the experimental team for two years, and it was only in the third year of work that the author was joined by two more experimental researchers, increasing the pace of work tremendously. For this reason, it has regrettably not been possible due to time constraints to achieve the initial goal of trapping within 4 years, so experimental results are limited and instead the focus is on the required preparations to build and assemble the Geonium Chip, with the goal of observing a single electron in a chip-based Penning trap.



(a) (b)

(c) (d)

FIGURE 1.4: To give the reader an idea of the extent of set up undertaken in this thesis, a selection of photographs were taken during the un-boxing and assembly of the lab. 1.4(a) shows the un-boxing of the *Sumitomo Heavy Industries SRP-062B* cold head, central to the experiment. 1.4(b) shows the un-boxing of the vacuum pump accessories. 1.4(c) shows the assembly of one of the workstation computers used in the lab for FEM and 3D design work. 1.4(d) shows the first trial assembly being prepared for vacuum seal testing.

Chapter 2

Theoretical Basics

2.1 The Ideal Penning Trap

This section deals with the theory associated with a the ideal Penning trap, used to understand the principles behind the operation of the 'Geonium Chip'. In reality, physical constraints and imperfections limit the accuracy attainable in a real-world trap.

The Penning trap differs from radio frequency or 'Paul' traps (named for Wolfgang Paul who shared the 1989 Nobel prize) in that it relies on a static electric $\vec{E}$ and magnetic $\vec{B}$ field arrangement to provide the trapping potentials. If one wanted to trap a particle in space using solely electric fields, the divergence of the electric field $\vec{\nabla} \cdot \vec{E}$ (and hence the divergence of the force on the particle) must be negative, that is to say, point towards the trapping region from all directions. Since this would violate Gauss's law which states the divergence of any electric field in free space is always zero, no solutions of the static potential Φ exist such that it is possible to solve the Laplace equation in free space

$$\vec{\nabla}\vec{E} = \vec{\nabla} \cdot (-\vec{\nabla}\Phi) = -\nabla^2\Phi = 0 \tag{2.1}$$

This means that only saddle points are able to be created solely with time-invariant electric or magnetic fields. It is therefore necessary to apply a restoring force along the potential maximum direction of the saddle point - in our case the x and y directions. In the Penning trap this takes the form of a magnetic field $\vec{B} = B_0\hat{z}$ in the direction of the z axis, and the resulting restoring force becomes

$$\vec{F} = q(\vec{E} + \vec{v} \times \vec{B}) \tag{2.2}$$

From the cross product it can be seen that a $\vec{B}$ in the direction of z yields a force orthogonal to z and the direction of the particle velocity $\vec{v}$. When the particle travels in the x direction, when it would otherwise be lost in absence of $\vec{B}$, it experiences a force which steers it back towards the trapping region, giving rise to a circular motion in the xy plane, and hence confinement is achieved. The frequency of this motion in absence of electric fields known as the free cyclotron motion ω_c is purely a function of the mass, charge and magnetic field

$$\omega_c = \frac{qB}{m} \tag{2.3}$$

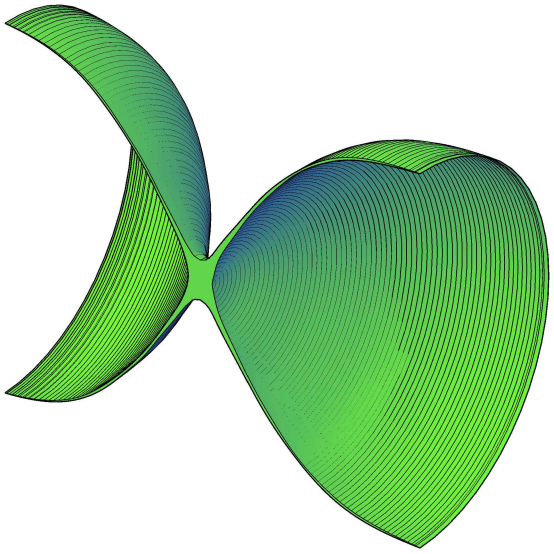


FIGURE 2.1: Shown is a cutaway of the basic shape of an ideal quadrupole potential in a non-elliptical Penning trap (the electrodes are not shown). Hyperbolic (2.2(a)) traps aim to mimic the surface curvature with the electrode shape, while cylindrical (2.2(b)) recreate the curvature using additional electrodes.

When the electrostatic and magnetic fields are combined, the trapped particle exhibits three distinct motional frequencies. The axial motion along the z axis of the trap, ω_z, is within the minimum of the electrostatic saddle potential supplied by the electrodes, and is ideally a harmonic motion. The radial confinement from the magnetic field gives rise

to the reduced cyclotron frequency ω_+, which is a modified version of the free cyclotron frequency in 2.3, and the interaction between the electrostatic and magnetic fields results in the magnetron frequency ω_-. The three frequencies are interlinked, and can be related by the invariance theorem [40]

$$\omega_c = \sqrt{\omega_+^2 + \omega_z^2 + \omega_-^2} \tag{2.4}$$

For a trap with rotational symmetry, that is to say a non-elliptical trap, the reduced cyclotron and magnetron motions can be expressed as

$$\omega_{+(non-elliptical)} = \frac{1}{2}(\omega_c + \omega_1) \tag{2.5}$$

$$\omega_{-(non-elliptical)} = \frac{1}{2}(\omega_c - \omega_1) \tag{2.6}$$

Where $\omega_1 = \sqrt{\omega_c^2 - 2\omega_z^2}$

2.1.1 Hyperbolic and Cylindrical Traps

Previous successful Penning trap designs use a rotational symmetry, for example a hyperbolic electrode shape [25], with the electrode surface following the equipotential surface of an ideal quadrupole to provide the electrostatic trapping. The advantage of this design is that a harmonic trapping potential could be made from just three electrodes, the central 'ring' and two 'end caps'. However, hyperbolic electrodes are not trivial to manufacture, and obscure line of sight to the trapping region. To simplify construction a cylindrical design was proposed featuring a tubular shape [41], which in addition to simplifying construction, gave easier access to the confined particle, and allowed for shuttling along the z axis between adjacent traps. The cylindrical arrangement can only achieve accurate measurements with the addition of two 'correction' electrodes, which, properly tuned, can correct for the anharmonicity introduced by the electrode shape. Cylindrical traps have been used in a variety of applications including bound-state QED experiments [27].

(a) (b)

FIGURE 2.2: Some example Penning trap designs: 2.2(a) is an example of hyperbolic Penning trap electrodes. This or a similar trap is used by the group of *L. Schweikhard, University of Greifswald* to perform laser spectroscopy experiments [5, 6] and features an optical access port in the ring. 2.2(b) is a cylindrical arrangement of multiple Penning traps used at *University of Mainz* for g-factor measurements of hydrogen-like ions, [7, 8] and more recently, variations of this trap type have been used for bound-electron magnetic moment experiments [9], and measurements of ions in extreme laser fields [10, 11].

2.1.2 Planar Penning traps

The planar Penning trap, i.e. a trap where the electrodes are confined to a single plane or surface, was motivated by the desire to use trapped electrons as building blocks for a quantum processor [42, 43] and a planar version of the Penning trap was first proposed in 2005 by S. Stahl [44]. The design was implemented [45] and improved [46], though as of writing this thesis, they have been unable to replicate the accuracy of 3D traps required to resolve an individual electron.

In general, planar traps are attractive because the designs allow for miniaturisation beyond what is achievable with a cylindrical or hyperbolic design, such as has been achieved in cold-atom chips and BEC chips. While a cylindrical trap may have many individual Penning traps [36, 37], the physical bulk of the electrodes mean that the trap length scale remains on the order of centimetres. It is conceivable that a planar design with true scalability could allow for arrays of tens if not hundreds of devices [47], if it was desired for a quantum processor application.

The proposed designs in these examples are rotationally symmetric about the z-axis, and are designed to be non-elliptical. The magnetic field is orientated such that it is normal to the electrode surface, allowing for equal potential landscapes in the x and y directions as would be found in a conventional 3D trap. This however means that

the potential along the z axis is more difficult to make harmonic, as the electrodes are asymmetric in z. This leads to uncertainty in the axial frequency ω_z.

The key difference between these designs and the 'Geonium Chip' experiment introduced in section 2.2 is that the Geonium Chip has a magnetic field orientation orthogonal to that of previous designs, with an arrangement mimicking the layout of a cylindrical trap. This allows the electrostatic potential in the z direction to be symmetric about the trapping region, giving a well defined axial frequency - crucial for single electron resolution. This however means that the x and y symmetry is broken, and hence the trap must be treated as elliptical and obeys the mathematics discussed in 2.2.3. Another benefit of this magnetic orientation is that it lends itself to shuttling of particles between adjacent trapping sites, such as is routinely done in cylindrical traps with multiple Penning trap regions [36, 37], a task which becomes significantly more difficult when trying to move orthogonally to the field orientation [48]. The first generation Geonium Chip detailed in this thesis contains one trapping site with 5 trapping electrodes, but there is no physical or technical reason why the chip could not contain any number of trapping sites and electrode arrays, scaled down in size.

Orientating the magnetic field and the electrodes this way means that the Geonium Chip does not have any rotational symmetry, and as a result the Geonium Chip is an elliptical Penning trap, and is thus subject to the mathematics associated with elliptical Penning traps detailed in 2.2.3.

2.2 The 'Geonium Chip'

As stated in section 2.1.2 the Geonium Chip is a 'planar' Penning trap, and attempts to replicate all of the functionality of traditional Penning trap designs while having a compact and scalable form factor. This is achieved by confining the electrodes of the trap to a single two-dimensional plane, hence the name 'planar'. This breaks the symmetry of the trap. Depending on the electrode projection taken this will either be the symmetry in the xy plane, or as is the case for our trap, the rotational symmetry that a cylindrical or hyperbolic trap has about its z axis. Without additional electrodes, this break in symmetry prevents the formation of an electric quadrupole, and hence trapping is not possible. The extra electrodes could simply be a specific area of grounded conductor, as

any charged particle - positive or negative - will experience an attractive force towards ground due to the potential difference between the charged particle and ground. It is hence possible to strategically place the ground plane of the electrode set up such that it completes the quadrupole once again, allowing trapping. A sketch of this is shown in figure 2.3.

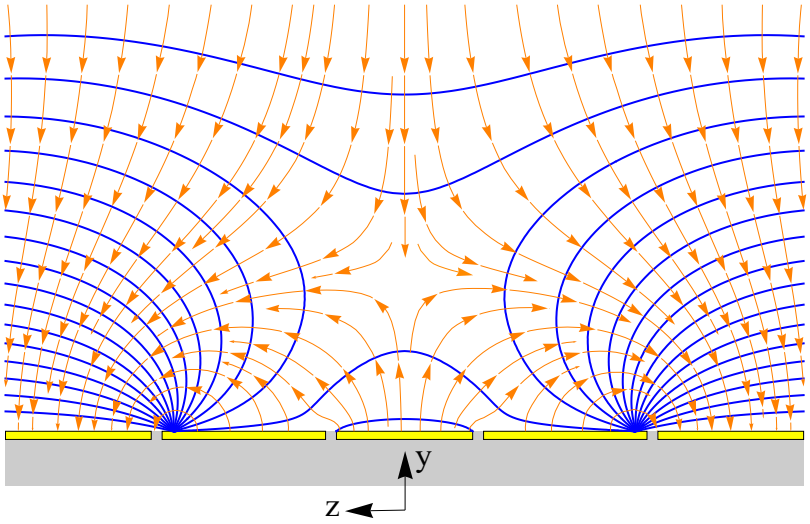


FIGURE 2.3: A sketch of how the Geonium Chip electric quadrupole is completed through the particles attraction to ground; this is the origin of the downward facing field above the trapping region y_0

In the 'Geonium chip' the trap is formed from a projection of the well-known cylindrical Penning trap [41] (shown in figure 2.4) [12], with the 5 electrodes - ring, upper correction and end cap, and lower correction and end cap - familiar to the cylindrical design. For this reason the electrode designation and orientation of the trap axes are the same, to make comparison between different Penning trap designs simpler. The quadrupole is completed by the grounded side planes, positioned to either side of the electrode array. This arrangement is similar in appearance to a coplanar wave guide, which led to early designs for the chip being known as 'coplanar wave-guide Penning trap', with the possibility of transmitting the microwave frequency ω_+ signal along the electrodes. It was chosen for the 1^{st} generation chip to detect the ω_+ signal via a separate near-field coupled wave-guide for simplicity. Future generations of the 'Geonium chip' may still utilize CPW this design. The ground plane immediately next to the trapping electrodes has been separated such that it will be possible in future to modify the potential landscape in the trap, enabling control of the ellipticity of the particle motions, and opening up options not available to non-elliptical traps, detailed further in section 2.2.4 [15].

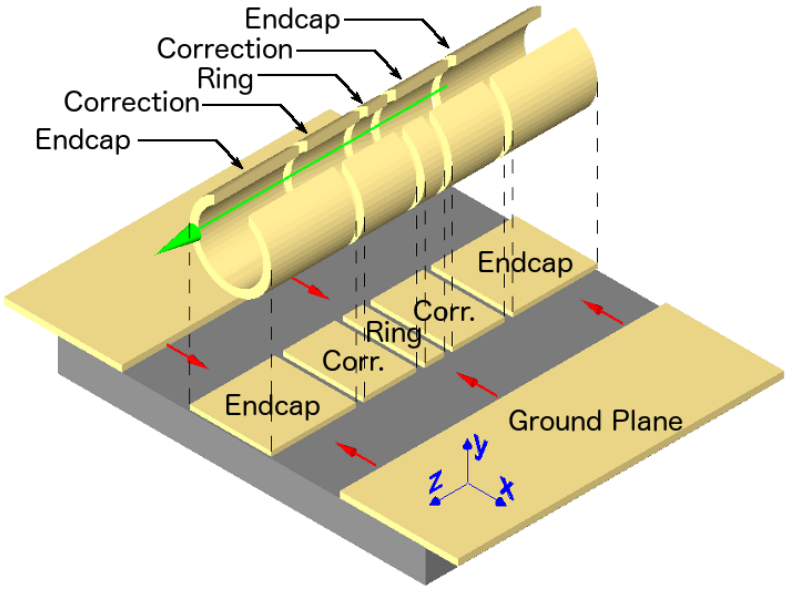


FIGURE 2.4: This graphic shows how the electrode structure is taken from the 2D projection of a cylindrical Penning trap. For familiarity, the axes orientation of x, y, z is kept the same, and is displayed on the figure, and will be referenced throughout this document when referring to the particle position and motions [12]. The magnetic field orientation is denoted by the green arrow along z.

2.2.1 Electric Potential

The electric potential in a Penning trap forms a potential minimum along the trap z axis, allowing confinement in the z direction. As stated in section 2.1, it is forbidden by Earnshaw's theorem (equation 2.1) to create a potential minimum in all three spatial dimensions simultaneously using static electric fields, so the electric potential takes the shape of a saddle, with a minimum in the z direction and a maximum in the x, y directions.

The ideal Geonium Chip trap is an elliptical trap and so follows the equations of motion detailed in section 2.2.3. The ellipticity ϵ represents the difference in potential curvature in the x and y directions, and is defined as

$$\epsilon = \frac{C_{200} - C_{020}}{C_{002}}. \tag{2.7}$$

With the curvature coefficients C_{ijk} defined as

$$C_{ijk} = \frac{1}{i!\,j!\,k!} \cdot \frac{\partial^{i+j+k}\,\phi(x,y,z)}{\partial x^i\,\partial y^j\,\partial z^k}\Big|_{(0,y_0,0)}. \tag{2.8}$$

The ideal potential is then

$$\phi_{quad} = V_r\, C_{002} \left(z^2 - \frac{x^2+(y-y_0)^2}{2} + \frac{\epsilon}{2}(x^2 - (y-y_0)^2) \right). \tag{2.9}$$

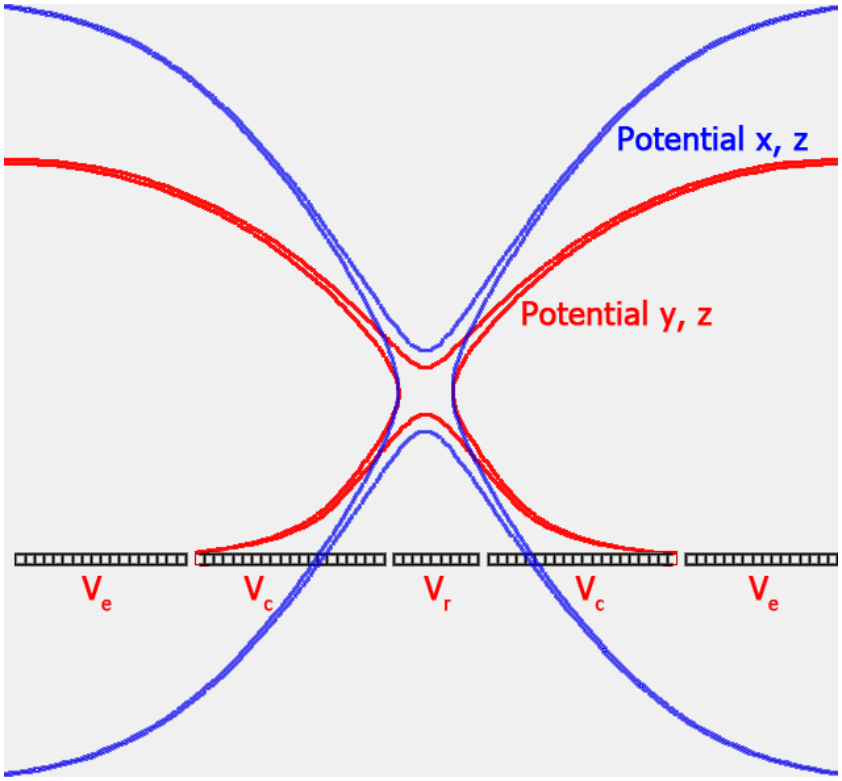
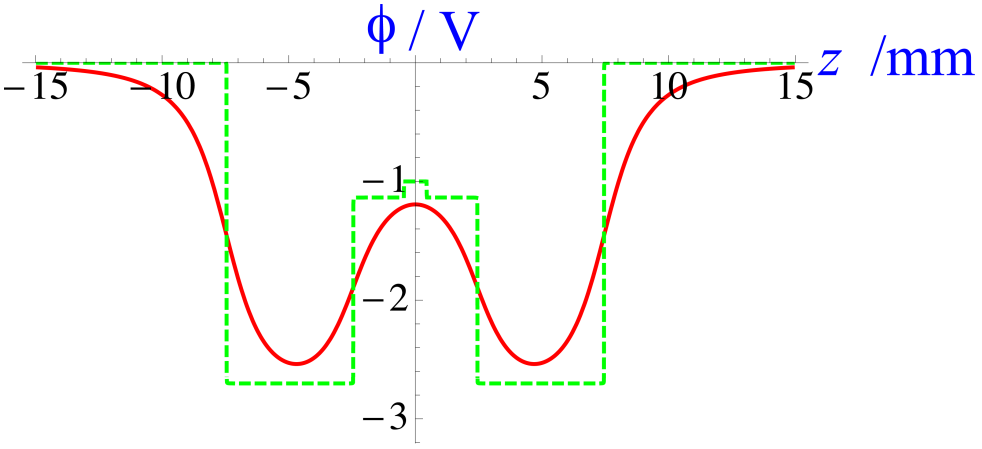


FIGURE 2.5: Shown are some example equipotential lines in the y, z plane of the Geonium Chip at $x = 0$, with the same equipotentials in the x, z plane at y_0 superimposed on the y, z potential. The diagram has no physical meaning, and serves only to illustrate the difference between C_{200} and C_{020}

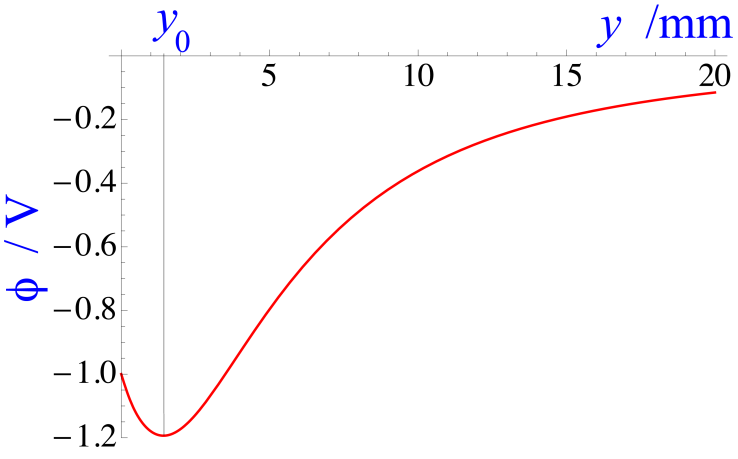
Calculation of the trapping potential can be done by summing the contributions from each electrode.

$$\phi(x,y,z) = V_r \cdot f_r(x,y,z) + V_c \cdot f_c(x,y,z) + V_e \cdot f_e(x,y,z) + f_{gaps}(x,y,z \,|\, V_r, V_c, V_e) \tag{2.10}$$

Where V_r, V_c and V_e is the DC voltage applied to the 'ring', 'compensation' and 'end-caps', respectively. The functions f_r, f_c and f_e are dictated solely by the dimensions of the trap - shown in figure 2.8 - and are independent of applied voltage. The electrodes are separated by insulating gaps, which make a contribution to the overall potential - the extent of which depends on the trap dimensions and the voltages applied to the electrodes. These contributions are accounted for by the term f_{gaps}.



(a)



(b)

FIGURE 2.6: Figure 2.6(a) shows the potential at the trap surface $y = 0$ in green dotted line, for electrodes with the dimensions listed in table 2.2 ($l_r = 0.9, l_c = 1.668, l_e =$ 5mm). The voltages listed in table 2.1 are negative, as the goal of the Geonium Chip is to trap electrons, and so the potential seen by the electron is inverted in y. The potential 'seen' at the position of the electron is overlaid in red and at this position can be seen to be smooth and harmonic about $z = 0$. Figure 2.6(b) shows the shape of the potential in the y direction. The trapping position y_0 is marked at the equilibrium point

TABLE 2.1: Voltages used in the examples and simulations of the Geonium Chip

Electrode	Example Voltage (V)
Ring V_r	-1
Correction V_c	-1.046
End Cap V_e	-2.737
Tunable Ground V_g	0

Due to the x and z symmetry of the electrodes, the trapping region can be seen to be above the ring electrode in its exact centre, which has co-ordinates $x, z = 0$. All that is left to do to calculate the trapping height is to determine the equilibrium point where the field direction in the y axis reverses. This 'trapping height' will be referred to as y_0, expressed formally as

$$\frac{\partial \phi\,(0, y, 0)}{\partial y}\Big|_{y=y_0} = 0 \tag{2.11}$$

Assuming the contribution of the gaps is small enough, that is to say $f_{gaps} \to 0$ (see reference [12] for a full discussion), then dividing equation 2.11 by the voltage on the ring electrode expresses the trapping height relative to the ring voltage, in the form of the ratios $T_c = \frac{V_c}{V_r}$ and $T_e = \frac{V_e}{V_r}$. The advantage of this is that once an optimal ratio has been calculated, the ring electrode voltage can be altered to a new value and optimal trapping height will be already calculated.

$$\frac{\partial f_r}{\partial y}\bigg|_{y=y_0} + T_c \cdot \frac{\partial f_c}{\partial y}\bigg|_{y=y_0} + T_e \cdot \frac{\partial f_r}{\partial y}\bigg|_{y=y_0} = 0 \tag{2.12}$$

The voltage ratios T_c and T_e have important consequences for the particle and the accuracy of measurement. The ratio T_e mainly defines the trapping height of the electron y_0, and is shown in figure 2.7(a). T_c serves to eliminate the dependence of the axial frequency on the energy of the particle, by smoothing out anharmonicities in the potential.

The layout symmetry also implies that any value of C_{ijk} with either odd i, odd k or both, would be invalid and hence vanish. This simplifies calculation of higher order anharmonicities in the potential, and the Taylor expansion of the potential (up to the 4^{th} order) around the trapping region reduces to

$$\begin{aligned}\phi(x, y, z) &= \phi(0, y_0, 0) + \ldots\ldots \\ &+ \underbrace{C_{002}\, z^2 + C_{200}\, x^2 + C_{020}\,(y - y_0)^2}_{\phi_{quad}} + \underbrace{C_{012}\, z^2 (y - y_0) + C_{210}\, x^2\,(y - y_0) + C_{030}\,(y - y_0)^3}_{\text{odd anharmonicities}} \\ &+ \underbrace{C_{202}\, z^2\, x^2 + C_{022}\, z^2\,(y - y_0)^2 + C_{220}\, x^2\,(y - y_0)^2 + C_{004}\, z^4 + C_{400}\, x^4 + C_{040}\,(y - y_0)^4}_{\text{even anharmonicities}}.\end{aligned} \tag{2.13}$$

The ratio T_c is the ratio of correction to ring voltage, and there exists an optimised voltage ratio T_c^{opt} whereby the two most significant curvature coefficients for the axial mode C_{004} and C_{012} - which are in general non-zero - are such that their energy dependent

contributions to the axial frequency are equal and opposite, cancelling each other, and eliminating the axial frequency dependence on energy $\Delta\nu_z/\Delta E_z$. As T_e and hence y_0 is altered (figure 2.7(a)), a new value of T_c^{opt} must also be found, shown in 2.7(b). However, a value of T_c^{opt} does not always exist, and outside of the range of y shown in 2.7(a) it cannot be optimised, the effects of the anharmonicities are too large, and accurate measurement is not possible. This range is known as the 'useful trapping interval' [12] and is the region where for a given geometry, particles can be observed with accuracy. The variation of T_c^{opt} with trapping height y_0 is shown in figure 2.7(b). An optimal trapping height y_0^{012} does exist for the trap geometry, where the values of $C_{004} = C_{012} = 0$, which would be the ideal trap. However this limits flexibility, and is not necessary for accurate measurement.

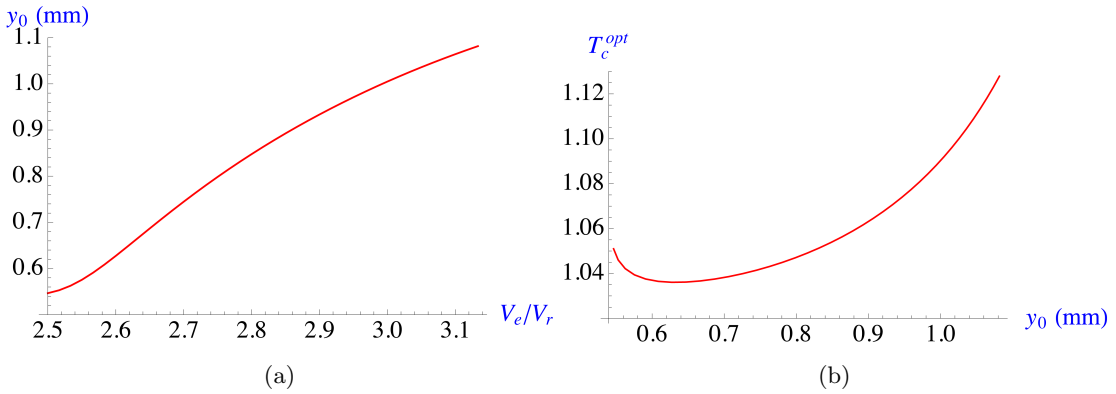


FIGURE 2.7: Figure 2.7(a) shows the dependence of the trapping height y_0 on the end-cap tuning ratio T_e. Figure 2.7(b) shows the variation of the optimal value of T_c as the trapping height y_0 is varied.

TABLE 2.2: Dimensions of the first generation Geonium Chip

Dimensions of the 1^{st} generation Geonium Chip	
Dimension	Length
S_0	7.000mm
S_1	3.000mm
l_r	0.900mm
l_c	1.668mm
l_e	5.000mm
η_1	0.010mm
η_2	0.010mm

The main shape of this saddle is provided by the 'end cap' and 'ring' electrodes, however the potential generated by a three electrode set up is highly anharmonic, resulting in

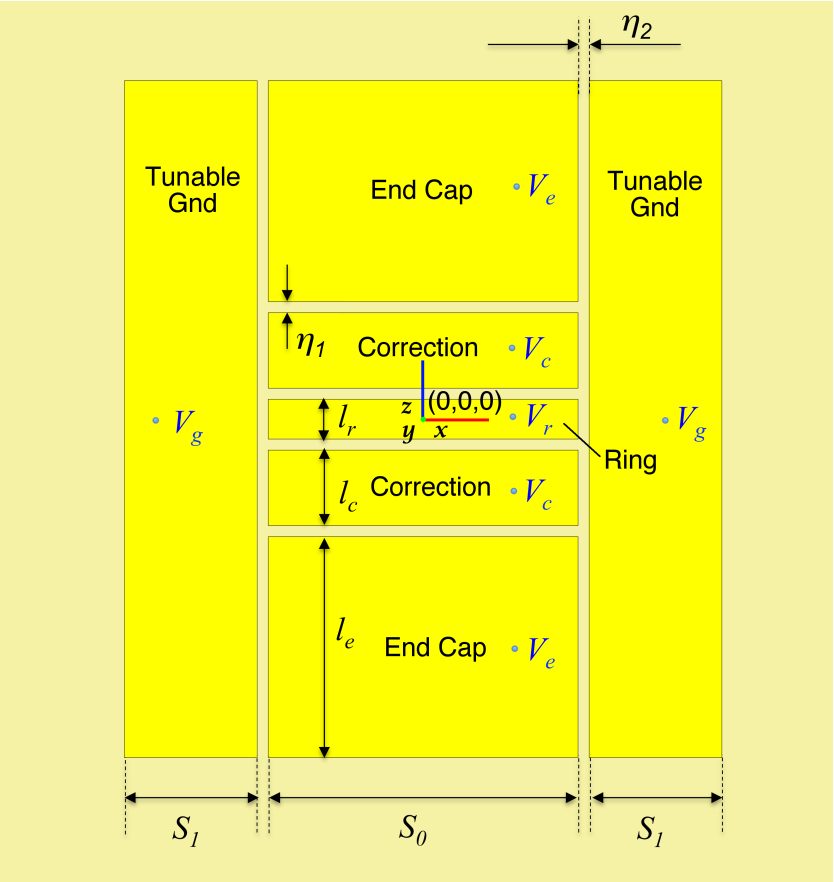
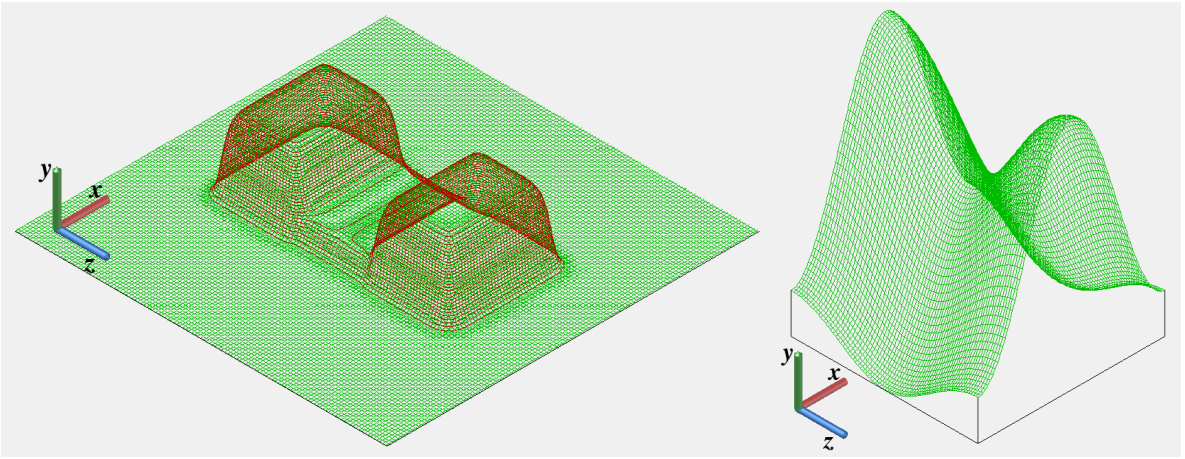


FIGURE 2.8: A sketch of the electrodes which provide the trapping potential for the Geonium Chip, to illustrate the dimensions used for the calculation of the potential. The co-ordinate origin $(0, 0, 0)$ lies on the centre of the 'ring' electrode surface, directly below where the trapping region is located. The dimensioning is for a general formulation of the Geonium Chip design, the first generation chip has the dimensions listed in table 2.2

poor frequency precision, and so it is necessary to add 'correction' electrodes which serve to modify the potential curvature so that, at the position of the particle, it is harmonic.

When electrostatic potential is superimposed on the magnetic field, as is the case in a Penning trap, the interaction gives rise to a motion in the trap in the xy plane, precessing around the $(0, y_0, 0)$ position with a frequency ω_-, known as the magnetron motion. The motion is heavily influenced by the ellipticity ϵ, so in a non-elliptical trap the magnetron motion is circular. In the Geonium Chip, the ellipticity can be manipulated so that the elliptical axes are very exaggerated and almost two-dimensional, as discussed in section 2.2.4. The motion follows the equipotential lines around a central point with higher potential energy (figure 2.22), known as a potential 'hill'. A sketch of this is shown in figure 2.11, which is intrinsically unstable and behaves differently to the other motional frequencies; cooling the particle causes a larger motional amplitude - the opposite of the



(a) (b)

FIGURE 2.9: Figure 2.9(a) shows a map of what the Geonium planar trap potential landscape looks like when calculated close to the chip, while figure 2.9(b) displays the saddle shaped potential when seen at the trapping height y_0

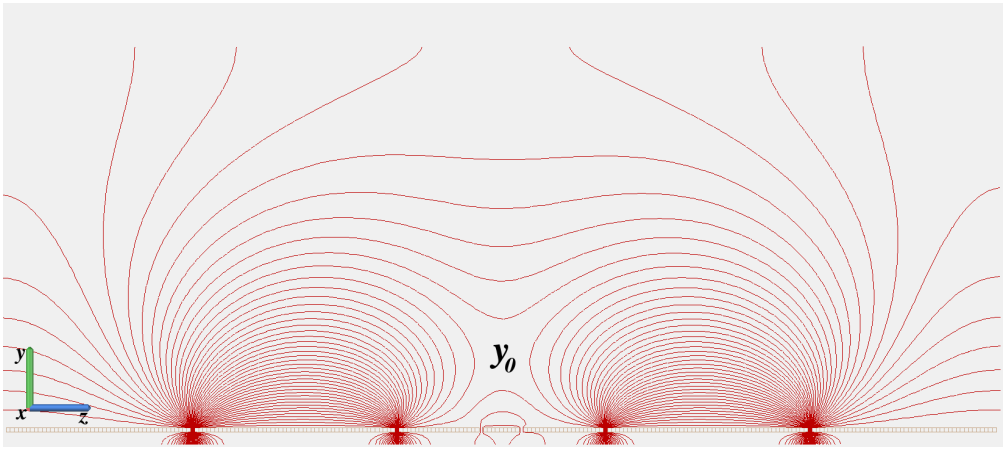


FIGURE 2.10: Equipotential lines along the z axis for the Geonium chip (with dimensions listed in 2.2) viewed at x_0, i.e. the centre line and trapping position. The quadrupole can be seen above the ring electrode, the centre of which dictates the trapping height y_0

cyclotron and axial modes. This is because the energy level of the magnetron mode is inverted [13], which can be thought of as having a *negative* energy level, and so therefore, in order to cool this mode energy must be *added* to it, in order to lift the electron up the potential hill, into a motional state with smaller amplitude.

2.2.2 Frequency Shifts and Anharmonicities

Evaluating equation 2.13, it is apparent that the higher order components in addition to the ideal quadrupole potential need to be taken into account. The components with

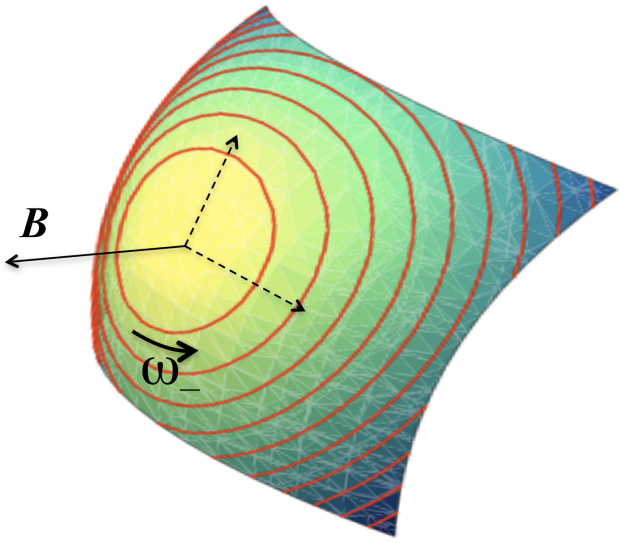


FIGURE 2.11: A sketch of the potential 'hill' which gives rise to the magnetron drift. To cool the mode, energy must actually be given to the system, raising the particle up the potential 'hill' into a smaller amplitude motion [13].

the biggest influence on the particle frequencies are the 3^{rd} and 4^{th} order terms, that is, terms with $3 \leq i+j+k \leq 4$. These terms cause the motional frequencies of the particle to be dependent on the particle energy. The shifts are linear, and the dependence can be expressed as a frequency shifts matrix M

$$\begin{pmatrix} \Delta\nu_p \\ \Delta\nu_z \\ \Delta\nu_m \end{pmatrix} = M \cdot \begin{pmatrix} \Delta E_p \\ \Delta E_z \\ \Delta E_m \end{pmatrix} = \underbrace{\begin{pmatrix} M_{1,1} & M_{1,2} & M_{1,3} \\ M_{2,1} & M_{2,2} & M_{2,3} \\ M_{3,1} & M_{3,2} & M_{3,3} \end{pmatrix}}_{M=\text{frequency-shifts matrix}} \cdot \begin{pmatrix} \Delta E_p \\ \Delta E_z \\ \Delta E_m \end{pmatrix} \tag{2.14}$$

For the Geonium Chip, it is crucial to measure the axial frequency ω_z with the greatest possible accuracy, as it is used in the determination of the cyclotron and magnetron frequencies, as well as being the primary frequency of interest for experiments such as the *continuous Stern-Gerlach effect* [8, 49] for non-destructive detection of the spin state of the particle.

This means that the matrix element of most importance to minimize is the $M_{2,2}$ element, that is, the element corresponding to $\frac{\Delta\nu_z}{\Delta E_z}$.

Each perturbation to Φ_{quad}, C^{ijk} listed in equation 2.13 contributes a matrix M^{ijk}, the sum of which form the overall frequency shifts matrix M (equation 2.15). In this way

each of the 3 odd and 6 even anharmonicities are countered, requiring a total of nine M^{ijk} matrices, and the overall frequency shifts matrix is

$$M = M^{012} + M^{210} + M^{030} + M^{220} + M^{202} + M^{022} + M^{004} + M^{400} + M^{040} \tag{2.15}$$

2.2.3 The Elliptical Penning Trap

In general, an elliptical trap is simply a trap where there curvature along the x and y directions are not equal, i.e. $C_{200} \neq C_{020}$. In the Geonium Chip all the electrodes are confined to a flat plane, and thus the x and y directions are asymmetric and it is an elliptical trap.

The motion of a particle in an elliptical trap has been calculated in detail by M. Kretzschmar [16], and tested experimentally by the same group for trapped argon ions, as well as for heavier fullerene molecular ions [14]. In these works it was shown that the theory calculated in [16] holds true for a real-world trap when the higher order deviations from the quadrupole described in section 2.2.2 are considered. The motional frequencies of the ideal elliptical trap (i.e. higher terms not considered) are

$$\omega_+ = \sqrt{\frac{1}{2}(\omega_c^2 - \omega_z^2) + \frac{1}{2}\sqrt{\omega_c^2\,\omega_1^2 + \epsilon^2\,\omega_z^4}} \tag{2.16}$$

$$\omega_- = \sqrt{\frac{1}{2}(\omega_c^2 - \omega_z^2) - \frac{1}{2}\sqrt{\omega_c^2\,\omega_1^2 + \epsilon^2\omega_z^4}} \tag{2.17}$$

$$\omega_z = \sqrt{2\,C_{002}\,\frac{q}{m}} \tag{2.18}$$

$$\text{with:} \quad \omega_1 = \sqrt{\omega_c^2 - 2\,\omega_z^2}.$$

In general, $\omega_+ > \omega_z > \omega_-$. For an electron in the Geonium Chip with 0.5 tesla magnetic field, the frequencies will be approximately

$$\begin{aligned} \omega_+ &= 2\pi \cdot \nu_+ = 2\pi \cdot 14 \text{ GHz} \\ \omega_z &= 2\pi \cdot \nu_z = 2\pi \cdot 26 \text{ MHz} \\ \omega_- &= 2\pi \cdot \nu_- = 2\pi \cdot 20 \text{ kHz} \end{aligned} \tag{2.19}$$

The axial motion ω_z is dependent on the curvature in the z-direction, C_{002}, with the curvature coefficients C_{ijk} defined in 2.8, and is thus determined by the trapping voltages chosen in the example. This allows flexibility, as the frequency can be adjusted as necessary. The trap depth of the Geonium chip with the example voltages in table 2.1 is around 1.13eV for singly charged ions (equating to a particle temperature of nearly 13,600K). For reference, the same voltage tuning ratios and magnetic field would trap a proton with the frequencies $(\nu_+^{\text{proton}}, \nu_z^{\text{proton}}, \nu_-^{\text{proton}}) =$ (7.6 MHz, 615 kHz, 20 kHz), with voltage polarities switched as appropriate. Heavier ions can still be trapped without modifying the trap depth, but may need parameter adjustment to bring the frequencies into more convenient ranges depending on application. For example hydrogen-like carbon as used in [50] would have frequencies of $(\nu_+^{^{12}C^{5+}}, \nu_z^{^{12}C^{5+}}, \nu_-^{^{12}C^{5+}}) =$ (3.1 MHz, 400 kHz, 20 kHz) or lower charged heavier ions e.g. $^{40}Ca^+$ (as used in [51]), with $(\nu_+^{^{40}Ca^+}, \nu_z^{^{40}Ca^+}, \nu_-^{^{40}Ca^+}) =$ (160 kHz, 97 kHz, 23 kHz). Reasons for choosing to raise the trap depth, might include raising the axial frequency ω_z into a frequency range with lower background noise, or to make it easier to detect electronically with conventional amplifiers. For the case of $^{40}Ca^+$ the optical transitions would allow for laser cooling (allowing extremely shallow trap depths if desired), as well as optical detection, so the electrical detection is less critical, however the frequencies in this example differ by only a few tens of kilohertz so it might be desirable to widen the difference between motional frequencies if this proved problematic.

The elliptical equations are mathematically the same as those of a basic Penning trap, but with an additional ellipticity parameter ϵ (equation 2.7). From equations 2.16 - 2.18 It is also possible to measure ϵ experimentally through the motional frequencies with

the following relation

$$\epsilon = \pm \frac{\sqrt{\left(\omega_+^2 - \omega_-^2\right)^2 - \omega_c^2\,\omega_1^2}}{\omega_z^2}. \tag{2.20}$$

To revert to the ideal non-elliptical equations 2.5 and 2.6 it is simply a matter of setting the ellipticity $\epsilon = 0$.

In the case of an electron in the Geonium Chip, the ω_+ lies in the microwave regime, and so it is intended for the Geonium Chip to be used in GHz frequency quantum applications, coupled through photons to circuit QED devices for example [52], electron spin devices [53, 54] [55] or other atomic or molecular systems [56, 57]. One of the primary goals of the Geonium Chip is to create a single-photon microwave sensor, capable of detecting individual microwave photons, as has been achieved in previous non-planar Penning traps [2]. This high frequency is only achievable with electrons, for example the reduced cyclotron frequency of a proton at the same 0.5 tesla field is $\nu_{+\text{proton}} = 7\text{MHz}$, thus to reach the GHz regime with a proton requires infeasibly large magnetic fields of many hundreds of tesla.

The motional amplitudes have been calculated as

$$\begin{aligned} A_+ &= \frac{1}{\omega_+}\sqrt{\frac{2E_+}{\gamma_+\, m}}\ , \text{ where } \gamma_+ = 1 - \frac{\omega_z^2}{2\,\omega_+^2} \simeq 1\,. \\ A_- &= \sqrt{\frac{2\,E_-}{(\omega_-^2 - \omega_z^2/2)\, m}}\,. \\ A_z &= \frac{1}{\omega_z}\sqrt{\frac{2\,E_z}{m}}\,. \end{aligned} \tag{2.21}$$

For an electron in the same example Geonium Chip trap, the largest amplitude of motion (after cooling is applied) is $A_z = 68\mu\text{m}$. A_- is next largest at around $3\mu\text{m}$, and the reduced cyclotron A_+ is just 128nm. The individual positional components x, y, z have also been calculated as a function of time [16] and are influenced by the ellipticity ϵ, which is manifest through the dimensionless coefficients $-1 \leq \xi_\pm,\ \eta_\pm \leq 1$ (equations 2.24, 2.23).

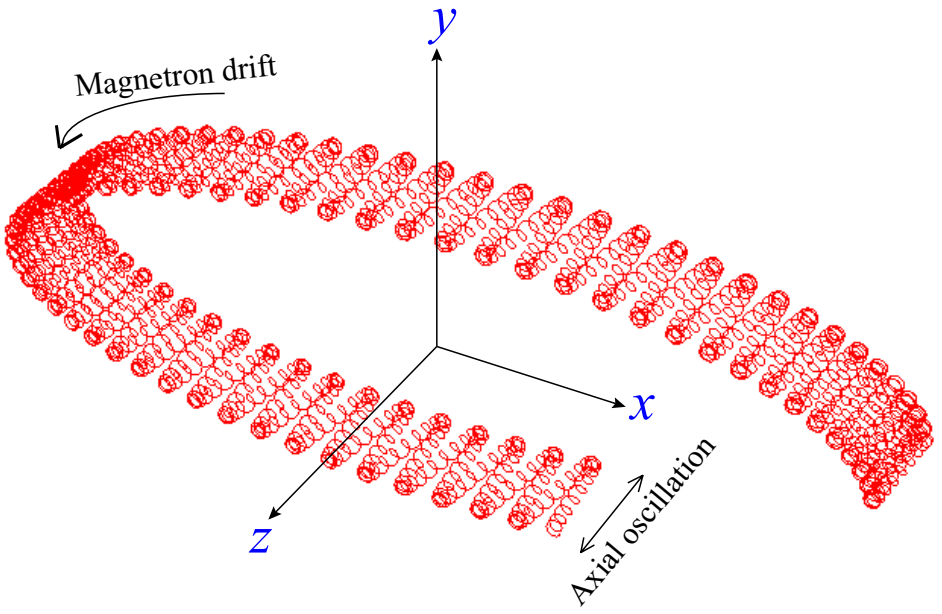


FIGURE 2.12: Shown is a diagram of the combined motions in an elliptical Penning trap. The amplitudes and frequencies have been exaggerated for clarity, as there are roughly three orders of magnitude difference in frequency between each. The fastest of the motions is the cyclotron frequency ω_+, which for an electron in a 0.5T field lies in the microwave regime at approximately 14GHz, and is seen as the tight loops along the particle path in the x, y plane. The axial motion ω_z is the sinusoidal motion in the z direction, and in the example Geonium Chip, lies in the radio frequency regime at approximately 26MHz. Finally the lowest frequency motion is that of the magnetron drift with a frequency ω_- of approximately 20kHz [12, 14].

$$\begin{aligned} x(t) &= \xi_+ \cdot A_+ \cos(\omega_+ t) + \xi_- \cdot A_- \cos(\omega_- t) \\ y(t) &= y_0 - \eta_+ \cdot A_+ \sin(\omega_+ t) - \eta_- \cdot A_- \sin(\omega_+ t) \\ z(t) &= A_z \cos(\omega_z t) \end{aligned} \tag{2.22}$$

$$\xi_\pm = \sqrt{\frac{\omega_c^2 + \epsilon\,\omega_z^2 \pm \sqrt{\omega_c^2\,\omega_1^2 + \epsilon^2\,\omega_z^4}}{2\,\omega_{+,-}/\omega_1 \sqrt{\omega_c^2\,\omega_1^2 + \epsilon^2\,\omega_z^4}}}. \tag{2.23}$$

$$\eta_\pm = \sqrt{\frac{\omega_c^2 - \epsilon\,\omega_z^2 \pm \sqrt{\omega_c^2\,\omega_1^2 + \epsilon^2\,\omega_z^4}}{2\,\omega_{+,-}/\omega_1 \sqrt{\omega_c^2\,\omega_1^2 + \epsilon^2\,\omega_z^4}}}. \tag{2.24}$$

These are known as normalized *semi-axes* in the x and y directions and refer to the major and minor axes of 'unit ellipses' i.e. ellipses with axes a, b equal to $(\eta_\pm) \cdot (1)$ and

$(\xi_{\pm}) \cdot (1)$ respectively [16].

2.2.4 Tunable Ellipticity and the Ultra-Elliptical Regime

As shown in figure 2.8, included in the Geonium Chip electrode layout are two isolated ground-plane electrodes, either side of the central electrode array. These are introduced fully in [15]. They have a corresponding ground plane tuning ratio $T_g = \frac{V_g}{V_r}$. In ordinary operation these are held in contact with ground at 0V, that is to say $T_g = 0$, however for special applications the voltage can be adjusted to alter the elliptical components of the potential landscape. In an elliptical trap the curvature of the potential in the x and y directions is intrinsically unequal, and so the ellipticity parameter ϵ (equation 2.7) is used to define the aspect ratio of the resultant motional ellipse. The orientation of the ellipse is dependent on the sign of ϵ. It is possible to trap with values of $|\epsilon| < 1$, that is $-1 < \epsilon < 1$. If ϵ is equal to or exceeds these limits, the magnetron motion becomes unbounded and hyperbolic, and trapping is not possible [16]. It can be seen in figure 2.13 that as $\epsilon \to 1$ the xy component of the motion becomes almost linear, with a very small minor axis (in this case y) amplitude. In this ultra-elliptical limit of $\epsilon \to 1$, the electron becomes confined to a quasi-two dimensional plane at $y = y_0$, and the magnetron frequency approaches 0Hz [14]. The ultra-elliptical limit opens up new areas of application by removing a degree of freedom from the particle for example the creation of a 2-dimensional electron gas in free-space, potentially mimicking 2DEG solid-state technologies [58]. These areas will be explored in further publications [15]. As it is not possible to apply magnetron side-band cooling without a well defined ω_-, it is necessary to apply magnetron cooling and then drive the motion as adiabatically as possible to $\epsilon \simeq 1$. In this regime, the reduced cyclotron frequency ω_+ reduces to the free cyclotron frequency ω_c, allowing direct observation of the the cyclotron mode. The particle is still trapped when close to this limit, but will be lost if ϵ ever becomes equal to or greater than 1. As the magnetron motion is not coupled to a detection circuit, the energy is essentially isolated from external fluctuations, and can be considered unchanging due to the long time constant associated with the extremely weak coupling to the environment [40]. However the particle is still sensitive to small perturbations in the trapping fields. Therefore it becomes more and more crucial to have no electrical noise sources as ϵ approaches 1. For the example used in figure 2.13, a fluctuation in T_g of 7×10^{-5} (corresponding to $\simeq 38$ µV for the most extreme example tuning ratio of $T_g = 1.829$)

will cause the magnetron motion to become unbounded, and the particle will be lost from the trap. The voltage sources (detailed in chapter 4.5) have a nominal stability of 1µV before filtering, therefore it is expected that stable trapping at this level of ellipticity is achievable. An optimised system could have voltage stability in the trapping potential of 10^{-8}, as has been demonstrated in [59].

It is important to note that the invariance theorem (equation 2.4 [40]) is still true for elliptical traps [16]. It is trivial to derive this using equations 2.16-2.18, and is true for all values of ϵ, even into the ultra elliptical regime as $\epsilon \to 1$.

The electrode configuration and geometry of the Geonium Chip mean that it is not possible to optimise a negative value of ϵ, that is to say one with a major axis aligned with the y axis of the chip. In theory though, other designs of geometries and electrodes could be employed to achieve this if necessary. This means that for the Geonium Chip, the ideal ultra-elliptical regime is for a positive value of $\epsilon \to 1$, aligned with the horizontal xz plane of the chip.

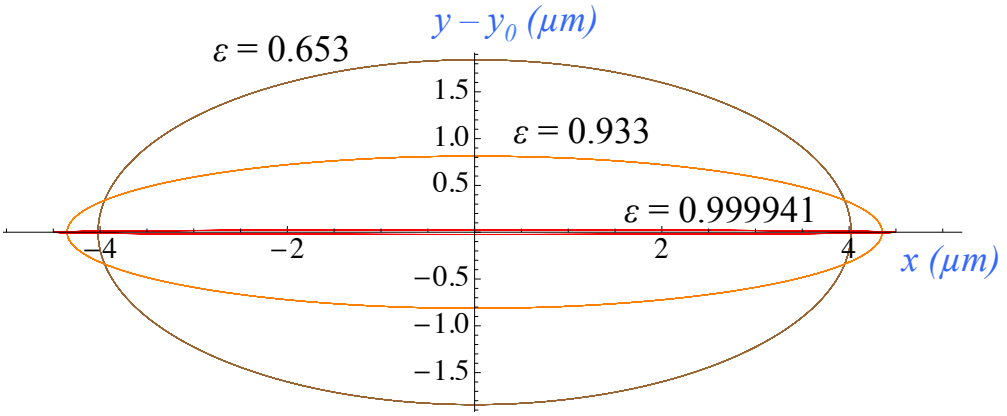


FIGURE 2.13: Simulated magnetron motions calculated from the equations of motion found in [15, 16] for $T_g = 0.522$, 1.653, and 1.829 giving $\epsilon = 0.653$, 0.933 and 0.999941 respectively. It can be seen that with an appropriate tuning ratio T_g, the y component of the magnetron motion can be all but eliminated.

As stated earlier in equation 2.20, the ellipticity can be measured experimentally, as it is a function of the motional frequencies in the trap [12].

In order to achieve very high ellipticity, such as the $\epsilon = 0.999941$ featured in figure 2.13, the magnetron mode must be cooled as detailed in [40]. If cooling is not applied, the the major axis of the ellipse extends out of the useful trapping region, into very anharmonic areas of the potential, where the shifts in frequency make it impossible to observe the particle.

The other use of the ground plane electrodes is to use the ratio T_g to correct for the 'natural' ellipticity, i.e. an ellipticity of $\epsilon = 0$, whereby the motional equations reduce to those of a non-elliptical trap, and all terms in the frequency shifts matrix 2.14 vanish. This could be of use in, for example, high precision mass spectrometry applications.

2.2.5 Calculating the Induced Currents

Since free electrons are not observable with visible light, the experiment uses no optics (with the exception of the photoelectric electron loading method), and all interactions and observations are carried out electronically. The electric field stemming from the charge of the electron displaces a corresponding charge on the electrode surface, analogous to charges on a capacitive plate, with one plate being the electron. The motion of the electron disturbs this charge in such a way that it is possible to measure the change of charge density on the electrode in the form of an AC signal with the frequencies of the electron motion, which can be then passed to the detection system, observing the electron in this way. This has a resistive effect on the electron expanded upon in section 2.2.6, which continues to sink its energy into the detection system until they are at thermal equilibrium.

To accurately predict the signal at the trap surface due to the particle motion, the induced charges are calculated via the Green's Function of the system $G(\vec{r}|\vec{r}')$ [17] for the Laplace equation with Dirichlet's boundary conditions

$$q_{\mathrm{ind}}(\vec{r}(t)) = -q \underbrace{\frac{1}{4\,\pi} \iint\limits_{\Sigma} dx'\, dz' \left.\frac{\partial\, G(\vec{r}(t)\,|\,x',y',z')}{\partial\, y'}\right|_{y'=0}}_{f_{\Sigma}(\vec{r})} \tag{2.25}$$

The surface of the integral Σ is the surface of the electrode designated as pickup electrode. The way which the pickup electrode is selected will be elaborated upon in section 2.2.7. The coordinate $\vec{r}$ is the source coordinate, and $\vec{r}(t)$ refers to the particle position at a given time t.

The appropriate Green's function for this system (assuming an infinite xz ground plane at $y = 0$) is [17]

$$\begin{aligned} G(\vec{r}\,|\vec{r}\,') &= \frac{1}{\sqrt{(x-x')^2+(y-y')^2+(z-z')^2}} \\ &- \frac{1}{\sqrt{(x-x')^2+(y+y')^2+(z-z')^2}}. \end{aligned} \tag{2.26}$$

Particle motion then gives rise to the induced currents on the surface of the electrode

$$I_{\text{ind}}(t) = \frac{dq_{\text{ind}}(\vec{r}(t))}{dt} = \vec{\nabla} q_{\text{ind}}(\vec{r}) \cdot \dot{\vec{r}}(t) = \frac{\partial q_{\text{ind}}}{\partial x}\dot{x} + \frac{\partial q_{\text{ind}}}{\partial y}\dot{y} + \frac{\partial q_{\text{ind}}}{\partial z}\dot{z}. \tag{2.27}$$

2.2.6 Resistive Cooling of the Axial Mode

As $I_{\text{ind}}(t)$ heads to ground through an impedance $Z(\omega)$, a voltage V_{ind} is seen across the impedance, sketched in figure 2.14. The charges induced on the electrode surface interact with the trapped electron via the induced voltage V_{ind}.

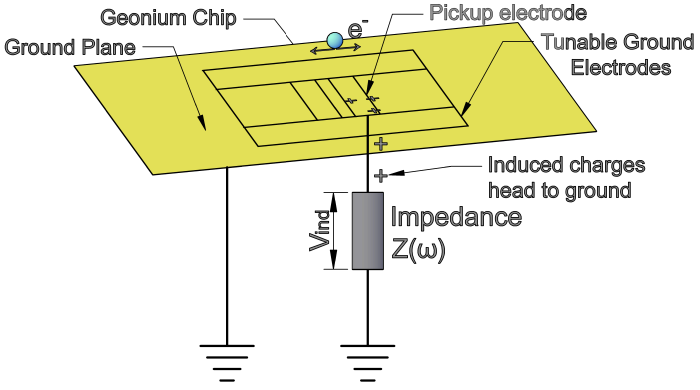


FIGURE 2.14: As the image currents go to ground, a voltage V_{ind} is seen across the impedance $Z(\omega)$

Using Green's second identity [17] the induced potential can be calculated as

$$\phi_{\text{ind}} = -\frac{V_{\text{ind}}}{4\pi} \iint_{\Sigma} dx'\, dz' \left. \frac{\partial\, G(\vec{r}(t)\,|\,x', y', z')}{\partial\, y'} \right|_{y'=0}. \tag{2.28}$$

By using equations 2.25 and 2.27, the induced potential can be written as

$$\phi_{\text{ind}} = -V_{\text{ind}} \cdot f_{\Sigma}(\vec{r}) = q\, Z(\omega) f_{\Sigma}(\vec{r})\, \vec{\nabla} f_{\Sigma}(\vec{r}) \cdot \dot{\vec{r}}. \tag{2.29}$$

where $Z(\omega)$ is the impedance of the detection system detailed in chapter 6 [60]. The voltage across the impedance (as shown in figure 2.14) is seen at the electrode. This generates an electric field $\vec{E} = \vec{\nabla}\phi_{\text{ind}}$, which interacts with the charge on the trapped particle and gives a corresponding force of

$$\vec{F}_{\text{ind}} = -q \cdot \vec{\nabla}\phi_{\text{ind}} = -q^2 Z(\omega) \cdot \vec{\nabla}\big\{ f_{\Sigma}(\vec{r}) \vec{\nabla} f_{\Sigma}(\vec{r}) \cdot \dot{\vec{r}} \big\} \tag{2.30}$$

This is the origin of the cooling force, which can be re-written as

$$\vec{F}_{\text{ind}} = -q^2 Z(\omega) \Big(\vec{\nabla} f_{\Sigma} \big(\vec{\nabla} f_{\Sigma} \cdot \dot{\vec{r}} \big) + f_{\Sigma} \big(\dot{\vec{r}} \cdot \vec{\nabla} \big) \vec{\nabla} f_{\Sigma} \Big). \tag{2.31}$$

where f_{Σ} is the individual contribution of the surface of the electrode Σ. Now it can be seen that $\vec{F}_{\text{ind}}$ is dependent on the particle velocity $\dot{\vec{r}}$ and acts to reduce the velocity and thus cool the particle [13, 61]. The energy is transferred to the detection system, where it is lost as heat through ohmic processes until the ambient temperature of the system is reached [62]. This is known as resistive cooling.

2.2.7 The Effective Coupling Distance

In order to calculate the coupling between the particle and the pickup electrode, and hence the rate at which the particle is cooled, the particle position is approximated to be the exact equilibrium position $(0, y_0, 0)$, as the particle motion is small compared to the size of the electrode. Making this approximation, known as the 'effective coupling

distance approximation' [60], the coupling can be represented by a distance vector $\vec{D}_{eff}^{-1}$ with the directional components

$$\vec{D}_{eff}^{-1} = \left(\frac{1}{D_{\text{eff}}^{x}}, \frac{1}{D_{\text{eff}}^{y}}, \frac{1}{D_{\text{eff}}^{z}} \right) \tag{2.32}$$

Defined as $\vec{D}_{eff}^{-1}(y_0; \Sigma) = \lim_{\vec{r}(t)\to(0,y_0,0)} \vec{\nabla} f_{\Sigma}(\vec{r}(t))$ The components D_{eff}^{i} have units of length, and so individually each $|D_{\text{eff}}^{i}|$ is an 'effective coupling distance', relating to the specific electrode dimensions Σ, and the equilibrium position y_0. In the case of the Geonium Chip correction electrode coupling to the axial motion, $|D_{\text{eff}}^{z}|$ is approximately 2mm. Physically, $\vec{D}_{eff}^{-1}$ is the normalised electric field produced by the electrode, as seen at the position $(0, y_0, 0)$

$$\vec{D}_{eff}^{-1}(y_0; \Sigma) = \frac{1}{1 \text{ Volt}} \vec{E}_{\Sigma}(0, y_0, 0)\,. \tag{2.33}$$

Using the effective coupling distance approximation, equation 2.31 reduces to

$$\vec{F}_{\text{ind}}(\omega) = -q^2\, Z(\omega)\, \vec{D}_{eff}^{-1} \cdot \left(\vec{D}_{eff}^{-1} \cdot \dot{\vec{r}} \right). \tag{2.34}$$

This 'self-force' [60] performs the resistive cooling upon the particle, and also couples the particle to detection system, whereby the particle currents drive the resonant impedance of the detection coil $Z(\omega)$. This leads to the detection signal V_{ind}.

$$V_{\text{ind}}(\omega) = -q\, Z(\omega)\, \vec{D}_{eff}^{-1} \cdot \dot{\vec{r}} \tag{2.35}$$

So then, it can be seen that as $\dot{\vec{r}}$ has components in all directions of space, the initially induced voltage V_{ind} would have contributions from all three trapping frequencies ω_+, ω_-, and ω_z. However the impedance $Z(\omega)$ is supplied by a tuned resonant LC circuit, and is strongly dependent on frequency. Thus it can be tuned such that voltage is detectable only at the resonant frequency of the LC tank-circuit, and signal with a frequency outside of the resonance width are below the system noise. For the main part of this thesis the main frequency of interest is the axial ω_z. The tank circuit for this mode takes the form of a helical resonator discussed in chapter 6.

From 2.34, a time constant τ^i can be derived in terms of the effective coupling distance and the impedance.

$$\tau^i(\omega) = \frac{m}{q^2} \cdot \frac{1}{Z(\omega)} \cdot \left(D^i_{\text{eff}}\right)^2 . \tag{2.36}$$

This time constant represents the rate at which the particle loses energy to the surrounding system, and it shows that for a given detection electrode and impedance, different degrees of freedom i cool at different rates depending on the square of D^i_{eff}. For this section, only the z degree of freedom will be considered, as coupling to the x and y is required only for the resistive cooling of the cyclotron and magnetron modes detailed in [60], and is beyond the scope of this thesis, and so from here onwards:

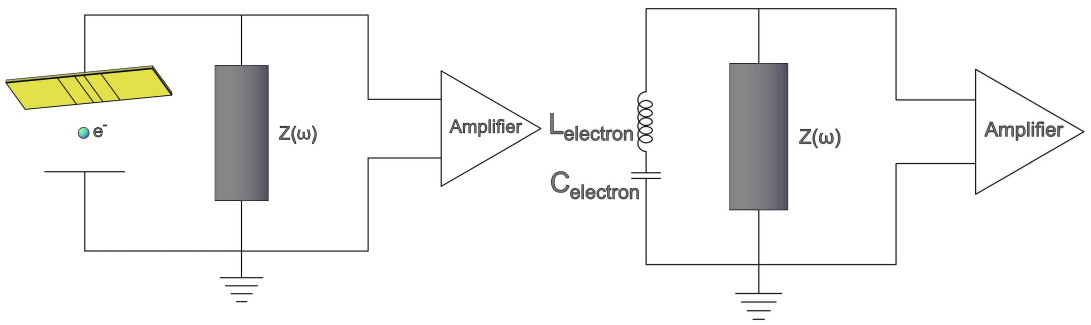
$$\tau^i(\omega) \rightarrow \tau^z(\omega_z) = \frac{m}{q^2} \cdot \frac{1}{Z(\omega_z)} \cdot (D^z_{\text{eff}})^2 \rightarrow = \tau$$

.

The Penning trap and electron together act as a capacitor, with an associated value of C, as well as a parasitic value of L as found in a real capacitor (see figure 3.11). The value of L is a function of the effective coupling distance and can be expressed as

$$L_{\text{electron}} = \frac{m}{q^2} \left(D_{\text{eff}}\right)^2 \tag{2.37}$$

This LC equivalence is sketched in figure 2.15. The series arrangement of the impedances L_{electron} and C_{electron} appears in parallel with the impedance $Z(\omega)$ as shown in figure 2.15(b).



(a) (b)

FIGURE 2.15: An electron suspended in a Penning trap 2.15(a) is equivalent to 2.15(b), a series LC circuit in parallel with the impedance Z(ω)

The values of L_{electron} and C_{electron} are related to the frequency of motion of the electron, in this case we are considering ω_z and it is equal to the resonant frequency of the equivalent LC circuit, $\omega_z = 1/\sqrt{L_{\text{electron}}C_{\text{electron}}}$. By rearranging equation 2.37, the relation to the detection circuitry time constant can be seen, $\tau = \frac{L_{\text{electron}}}{Z(\omega)}$.

2.2.8 LC Tank Circuit

The impedance $Z(\omega)$ is implemented in the form of a resonant 'tank' circuit, consisting of a parallel LC arrangement. In the case of the axial detection circuitry, this takes the form of a helical resonator with an inductance L_{coil} and parasitic capacitance C_{coil} such that the resonant frequency $\omega_0 = \omega_z$ i.e. $L_{\text{electron}}C_{\text{electron}} = L_{\text{coil}}C_{\text{coil}}$, as well as a resistance R_{coil} contributed by the system losses present in any real system. At resonance, the tank circuit contributes parallel resistance R_{p} [63]

$$R_{\text{p}} = \omega_0 LQ \tag{2.38}$$

Where Q is the quality factor (Q-factor) of the resonator defined as $\omega_0/\Delta\omega_0$, the width at half the maximum height of the resonance, and is a measure of the energy lost per cycle. The signal of the electron is very small, on the order of femtoamperes, so in order to obtain a readable signal at the input of the amplifier, the resistance R_{p} must be as large as possible in order to get a detectable voltage across it, in accordance with Ohm's law. Thus equation 2.38 dictates that the Q-factor should be designed to be as high as possible.

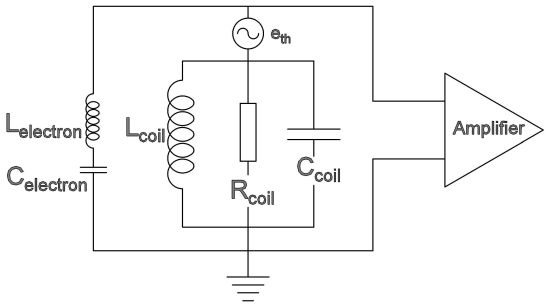


FIGURE 2.16: The equivalent circuit of the coupled tank circuit and electron. The system is driven by the thermal noise e_{th}

When in thermal equilibrium, the thermal Johnson noise of the system, represented in figure 2.16 as e_{th}, drives the circuit with thermal noise, and the resonance peak of the tank circuit can be observed. It appears as a peak because the impedance of this circuit appears as a maximum across the detection signal path. At the same time, the impedance of the confined electron appears as a minimum, shorting the spectrum to ground. This is simulated in figure 2.17.

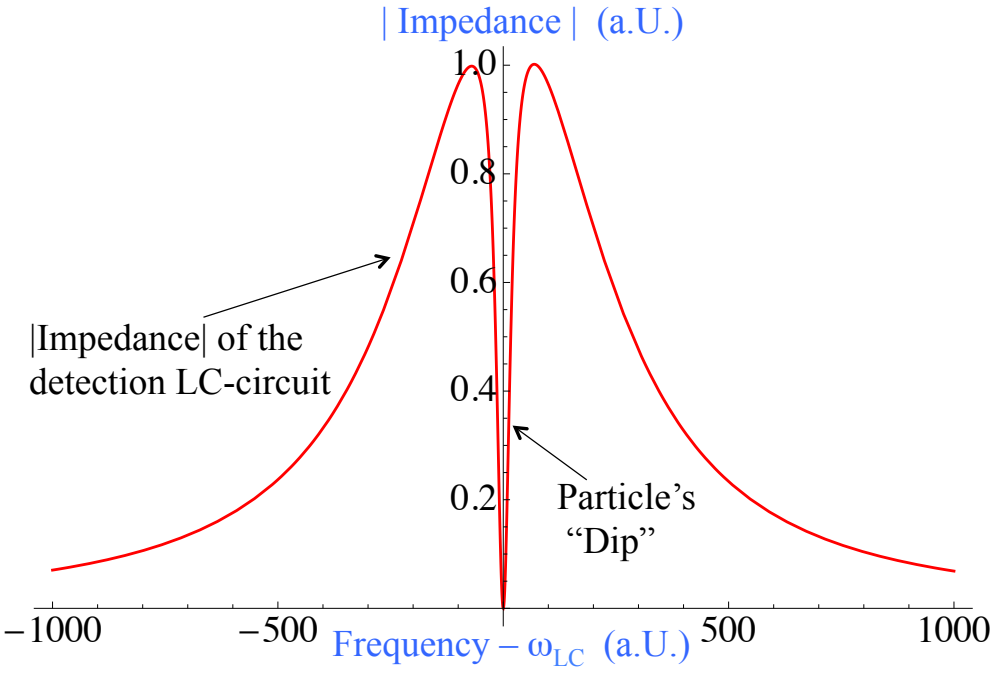


FIGURE 2.17: A simulation of the expected impedance spectrum and particle.

The width of this dip is given by $\Delta\omega = 1/\tau$ [61] and is an important parameter for a number of reasons. Firstly, the dip width is what makes the particle 'visible', and thus it is crucial that the dip is not so small that the particle dip is unresolvable. It is important then, that the time constant τ is as small as possible. Combing equations 2.36 and 2.38, we see that the time constant can be minimised by a maximum Q factor of the detection coil [64], as this dictates the parallel resistance R_{p} and a maximum coupling strength D_{eff} to the detection system.

$$\tau = \frac{m}{q^2} \cdot \frac{1}{R_{\text{p}}} \cdot (D_{\text{eff}})^2 = \frac{m}{q^2} \cdot \frac{1}{\omega_0 Q L_{\text{coil}}} \cdot (D_{\text{eff}})^2 . \tag{2.39}$$

Intuitively, the electron dip can be thought of as the resonance of a undamped LC circuit, with a width damping applied from the detection system. If there is no coupling, there

can be no damping and no dip is visible. So it is that the particle dip relies not only only the damping of the detection system, but also the coupling strength.

Estimates for τ can be made by using some example numbers for Q, and calculated values for L_{coil}, D_{eff} and ω_0, and for the Geonium Chip the cooling time constant can be expected to be on the order of a 1×10^{-3}s, for a relatively low tank circuit Q of around 550. With the same trapping voltages and a suitable coil (e.g. the coil used in [65]), a proton would have a cooling time constant on the order of a few tens of milliseconds for the axial mode, for a resonator Q of $\simeq$3000. These time constants reduce linearly with Q factor improvement, so with optimized resonators could potentially be reduced to a few hundred µs.

2.3 Magnetic Confining Field

In order for high measurement accuracy, the magnetic field must be as uniform as is possible, and non-varying in time. However, this is not strictly the case outside of certain boundary conditions, and is discussed in section 2.4.1. As mentioned in section 2.2.1 the electric potential only provides confinement along the z direction, the particle sees a potential maximum in the x and y directions and so to prevent the particle leaving the trap, a magnetic field is applied along the z axis. This generates a Lorentz force (equation 2.2), causing the particle to perform circular motion in the xy plane, and preventing particle loss in the x direction. If the electrostatic effects are ignored, the frequency of this motion depends only on the mass m, charge q and the magnetic field $\vec{B} = B_0\hat{z}$ (equation 2.3).

2.4 The Planar Magnetic Field Source

The magnetic field sources popular in previous Penning trap experiments are typically very large. These large-bore magnets have been used as they provide excellent field uniformity over a large area. In order to have a compact scalable system for the Geonium Chip, a radical new approach to the magnetics is proposed. The goals of fabricating a compact planar source are outlined in figure 2.18, with future generations of chip having designs incorporated into the micro-fabrication stages [66]. These sources are

designed to provide uniform field in the trapping region, and so the complexity of the problem reduces to one of smoothing the curvature through cancellation of the magnetic inhomogeneities detailed in section 2.4.1. A first prototype is described in section 7.

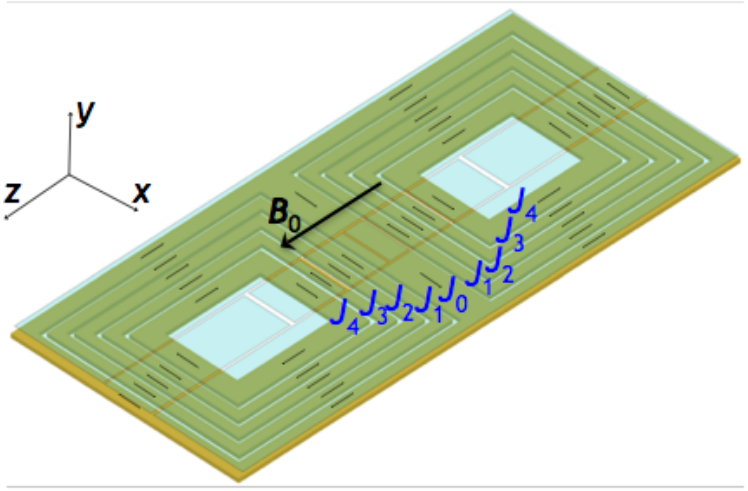


FIGURE 2.18: The conceptual design of a planar magnetic field source, with the currents $J_{0,1,2,3,4}$ necessary to correct for the field curvature present in a single wire source. For specific applications, this design also facilitates on-the-fly modification of the field, one example might be the generation of a temporary magnetic 'bottle'.

2.4.1 Magnetic Inhomogeneities

The principle behind the planar field source is that through the use of shim coils, wire geometries and current densities, solutions exist such that the fields from the shim coils cancel completely the inhomogeneity of the field from the main coil B_0. It has been shown that solving for one spatial direction simultaneously solves all other directions [15]. So then, the problem reduces to a one-dimensional problem, and in this section only corrections along the y axis will be considered. A similar approach is taken to that used in equation 2.13 for the electric field, but considering just one spatial direction. The expanded form of the field to the 4^{th} order is then

$$B_z = B_0 + B_{z,010}(y-y_0) + B_{z,020}(y-y_0)^2 + B_{z,030}(y-y_0)^3 + B_{z,040}(y-y_0)^4 + \dots \quad (2.40)$$

where the coefficients $B_{z,ijk}$ are defined by $B_{z,ijk} = \frac{1}{i!j!k!} \cdot \frac{\partial B}{\partial x^i \partial y^j \partial z^k}\big|_{(0,y_0,0)}$ and are the axial components of the magnetic field at the position of the particle y_0.

2.4.2 Solving for Currents

The magnetic field can thus be represented as the homogeneous field with a set of perturbations. The full solutions are quite mathematically involved and have been calculated in [15] and the patents [67, 68]. In this document then it is sufficient to say that it has been shown that solutions exist to neutralise the inhomogeneities, so the next step is to relate the desired fields to real world current densities. This is done through the matrix Γ where

$$\begin{pmatrix} J_0 \\ J_1 \\ J_2 \\ J_3 \\ J_4 \end{pmatrix} = \Gamma^{-1} \cdot \begin{pmatrix} B_0 \\ B_1 \\ B_2 \\ B_3 \\ B_4 \end{pmatrix} \quad \text{where:} \quad \Gamma = \begin{pmatrix} B_0^0 & B_0^1 & B_0^2 & B_0^3 & B_0^4 \\ B_{z,010}^0 & B_{z,010}^1 & B_{z,010}^2 & B_{z,010}^3 & B_{z,010}^4 \\ B_{z,020}^0 & B_{z,020}^1 & B_{z,020}^2 & B_{z,020}^3 & B_{z,020}^4 \\ B_{z,030}^0 & B_{z,030}^1 & B_{z,030}^2 & B_{z,030}^3 & B_{z,030}^4 \\ B_{z,040}^0 & B_{z,040}^1 & B_{z,040}^2 & B_{z,040}^3 & B_{z,040}^4 \end{pmatrix} \tag{2.41}$$

In this case $B_{z,ijk}^l = \frac{1}{i!j!k!} \cdot \frac{\partial B}{\partial x^i \partial y^j \partial z^k}\big|_{(0,y_0,0)}$ is the axial component for a given current density J_l with the stipulation that $J_l = 1$ at the trapping position $(0, y_0, 0)$. The solution is valid only for a specific value of y_0. If y_0 is to be modified, then the solution becomes invalid and must be recalculated for the new value and new values of J_l generated.

An example has been calculated, and is shown in figure 2.19. The result of this is that when the magnetic field components from each coil are added together, the field gradients are cancelled in the region occupied by the trapped particle, and the remaining magnetic field is homogeneous. If a trapped electron is cooled such that the motional amplitudes are small, i.e $A_z, A_- < 100\mu m$, then the electron never leaves the compensated region, giving the effect of a uniform magnetic field [15], using a compact planar source instead of a large solenoid. It can also be seen from 2.19 that the corrected field in all three spatial directions is much larger than the expected amplitudes of motion calculated in equations 2.21 for an electron at a temperature of 4K [12].

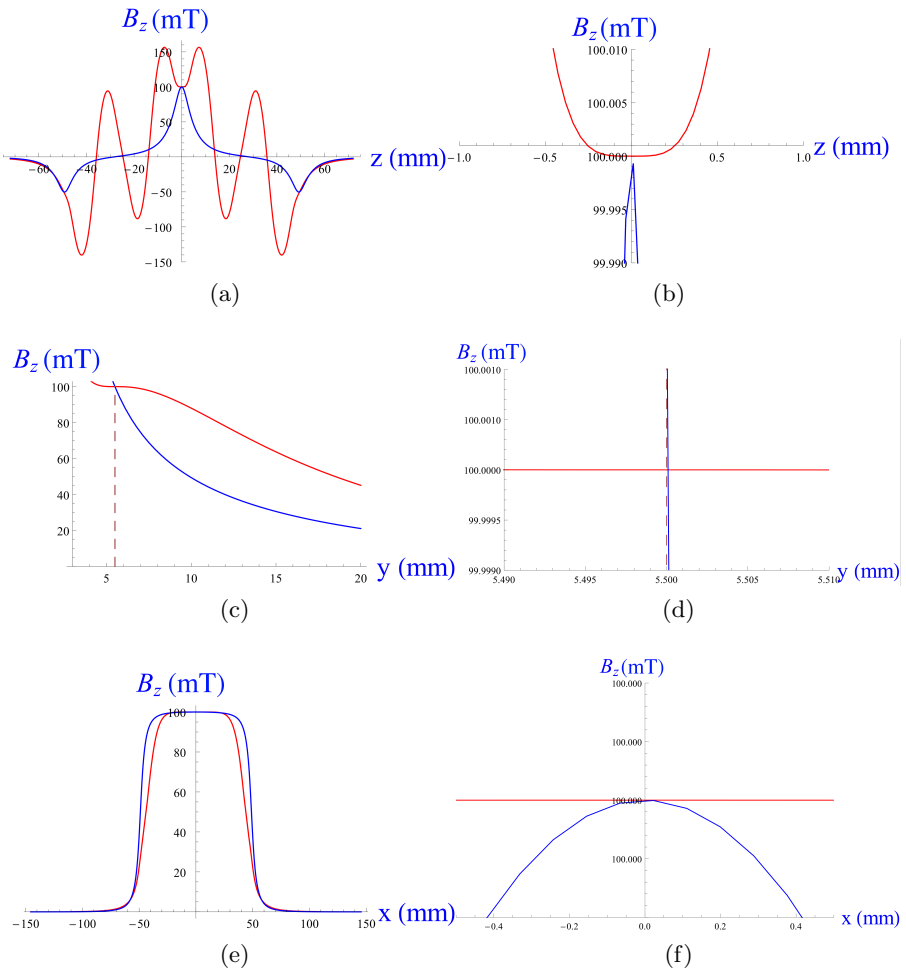


FIGURE 2.19: The z components of the magnetic field B_z for a field of $B_0 = 0.1\text{T}$ resulting from a single current source are shown in blue, while the shim corrected fields are shown in red. Variation of B_z with z is shown in 2.19(a), and 2.19(b) shows a close up of B_z around $z = 0$. Variation of B_z with y in 2.19(c), and x in 2.19(e). Outside of the trapping region, the fields can be quite eccentric, for example those seen in 2.19(a), but can be seen to flatten in the region of interest 2.19(b). The corrected fields have good homogeneity within a region of space large enough for cryogenic (i.e. low-amplitude) Penning trap experiments.

In the example presented in figure 2.19, the currents are as follows:

$$\begin{pmatrix} J_0 \\ J_1 \\ J_2 \\ J_3 \end{pmatrix} = \Gamma^{-1} \cdot \begin{pmatrix} 100\ \text{mT} \\ 0 \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} 103.193 \\ -106.240 \\ 111.560 \\ -104.695 \end{pmatrix} \cdot \frac{\text{A}}{\text{mm}^2} \tag{2.42}$$

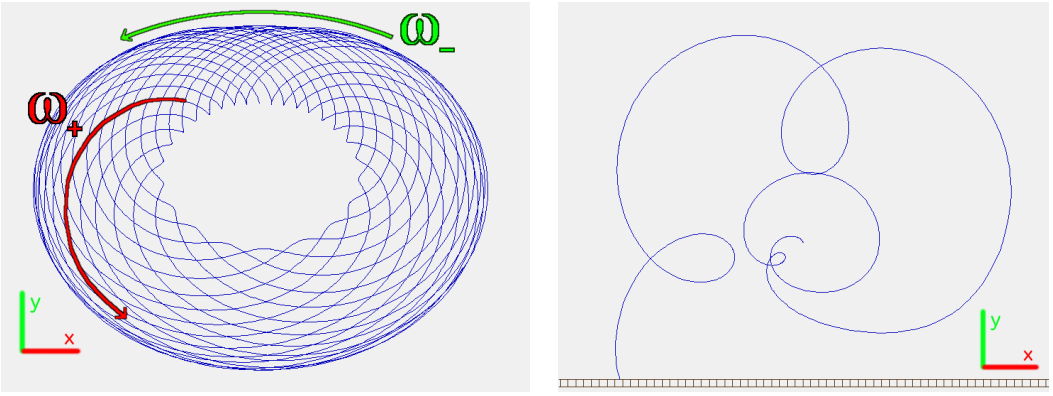
For the prototype coils detailed in section 7.1.1, the coil wires can be ideally wrapped with a density of roughly 5.42 conductors per mm^2. This means a 0.1T field can be

achieved with approximately 19-21A for 0.4mm insulated wire, which is large but within the range of what is achievable by the wire with appropriate current supplies.

If the case of 0.5T field is considered, then the current requirements jump by fivefold to

$$\begin{pmatrix} J_0 \\ J_1 \\ J_2 \\ J_3 \end{pmatrix} = \begin{pmatrix} 515.966 \\ -531.202 \\ 557.801 \\ -523.477 \end{pmatrix} \cdot \frac{\mathrm{A}}{\mathrm{mm}^2} \tag{2.43}$$

requiring an in-wire current of around 70A. If for the sake of argument the case of a 1T field is considered, it would require currents in excess of 200A, which although within limit of the current capabilities of the wire, would require expensive specialised current supplies, and additionally it be extremely difficult to manage the thermal effects of having such a high current flowing to the cryogenic region, as well as considerations from other effects like stray magnetic fields. As discussed in 4.3.3, there are NbTi wires available with diameters finer than 0.1mm [69], and the Geonium group are currently in talks with *Scientific Magnetics* to have coils wound with such a wire. This increases ideal packing density to around 63 conductors per mm^2 (for 0.1mm), and thus reduces current requirement to around 9.4% of the value needed for 0.4mm, to around 2A for a 0.1T field, or around 10A for 0.5T. At the time of writing, companies (for example *Supercon Inc.*) offer wires down to 25µm diameter - which would reduce current requirements to 0.5A for the case of 1T - however, using wires this width requires *thousands* of kilometres of wire to make the coil arrays and is thus infeasible for an array this size. Initially, for measurements focussing on proof of concept and on axial frequency precision, the Geonium chip can theoretically be operated accurately with magnetic fields as low as 10 mT, as the frequency of the axial mode is largely independent of the magnetic field. However, if the magnetic field becomes too small then the cyclotron amplitude A_+ becomes comparable to the magnetron amplitude A_-, and if the field and voltages are such that $\omega_c^2 \leq 2 \cdot \omega_z^2$, motion becomes unstable as equations 2.16 and 2.17 become unphysical [70].



(a) (b)

FIGURE 2.20: Simulations of the xy trajectory of an electron in the Geonium Chip with extremely low magnetic fields of 1.5 mT 2.20(a) and 1.4 mT 2.20(b), using the same example voltages as in table 2.1.

A potential downside to this planar method of B field generation is that the field is highly eccentric outside of the trapping region. This means the particles cannot be loaded from the z direction with the compensated field already in place, as the curvature of the field would steer the particles into the trap surface and walls before the trapping region is reached. Switching the magnetic field from some arbitrary non-ideal field, suitable for loading, to the compensated field suitable for analysis would take some finite length of time, making this field source less suitable for time-critical measurements such as particles with short lifetimes e.g. radionuclides with short decay times such as those used in [71–73]. This is particularly true if the method of 'flux pumping' (discussed chapter 7) is employed to generate the wire currents, as this method takes a comparatively long time to build the required fields. Another limitation is that, as the size of the homogeneous region of magnetic field is limited, it limits the amplitudes of particles that can be accurately observed. Particles with high energies or masses [74] would be unsuitable for this method of field generation, as the motion amplitudes could extend into the region of inhomogeneous magnetic field.

2.5 Particle Trajectory Simulations

To test the capabilities of the Geonium Chip, it has been modelled in the ion-optics software *SIMION*. This software served to provide a corroboration to the more mathematically rigorous results already calculated in *Wolfram Mathematica*.

SIMION simulates an electric field via an evenly spaced array of data points known as a 'potential array', the spacing of which should ideally be considerably less than the size of the smallest features in the model. Each point holds the potential data for that location. Unknown fields and potentials are extrapolated from the known points, and a smooth potential surface is generated [75]. Virtual particles are set up with initial conditions (energy, mass charge, position etc.), and the time evolution of the particles and hence trajectories can then be computed.

Setting an array of electrodes with the dimensions of the Geonium Chip, along with a superimposed magnetic field, allowed exploration of various scenarios quickly, for example the paths of the photoelectrons ejected, optimum injection points etc. as well as providing quick visualisation feedback of the effects on the characteristic trap motions, and example is seen in figure 2.21. With the software it was possible to simulate experimentally quantities such as maximum trappable electron energy, the effect of electrode switching, and the paths of trapped particles injected at various locations amongst other things.

TABLE 2.3: Comparison of SIMION and Mathematica calculated frequencies

Comparison of calculated frequencies for arbitrary test conditions of $V_r = -1$V, $V_e = -4$V, $T_c = 1.134$ and a magnetic field of $B_z = 1$T			
Frequency	Mathematica	SIMION	$\Delta\omega$
$\omega_+/2\pi$	27.99 GHz	28.03 GHz	+0.14%
$\omega_z/2\pi$	28.16 MHz	26.71 MHz	-5.1%
$\omega_-/2\pi$	12.97 kHz	12.19 kHz	-6.0%

A charged particle in uniform static $\vec{E}$ and $\vec{B}$ fields experiences a force in the direction of $\vec{E} \times \vec{B}$ [17], and thus the magnetron drift is expected to follow roughly along the equipotential lines of a given potential landscape [16]. An exploration of this, in the case of electrons in the Geonium Chip, can be seen in figure 2.22, as well as showing the limits of the magnetron motion. If the equipotential line forms a closed loop around the trapping region, then the particle is contained. If the equipotential line is open then the particle leaves the region and is lost to ground. As the distance from the trapping region $|y_{\text{in}} - y_0|$ increases, the magnetron orbits become increasingly eccentric until the particle is lost from the trap. As y_{in} approaches y_0 the orbits become more stable and regular.

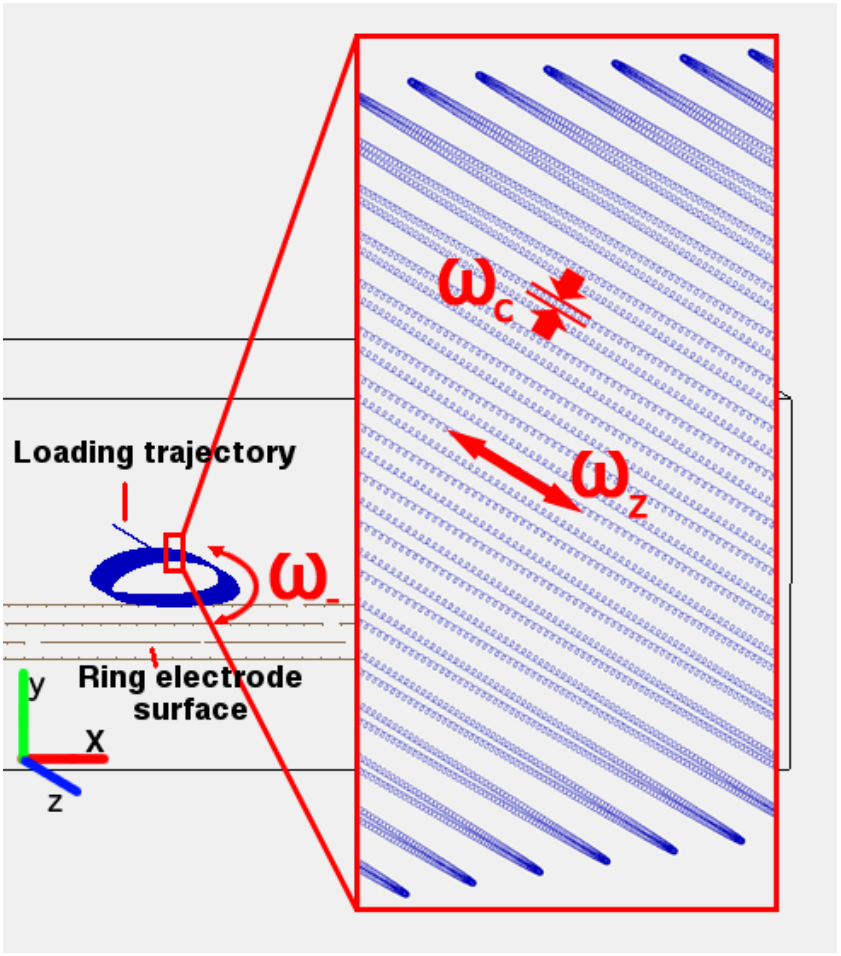


FIGURE 2.21: An example of a simulated electron confined in the Geonium Chip. At these extreme energies the magnetron and axial amplitudes dominate, and it is not possible to see the individual ion paths at this scale. Instead the ion path appears as a looped 'ribbon' with the width of the axial amplitude. Zooming in reveals that the electron is indeed exhibiting all three characteristic motions of Penning trap confinement.

2.5.1 Electron Loading

The loading of the electron is performed by ejecting electrons via the photoelectric effect from the metallic surfaces in the chamber, and from the trap electrodes. As the voltage on the electrodes can be switched quickly (limited to around 20µs by the DC low-pass filters), the task was then reduced to finding the best method of applying the magnetic field, as any changes to the magnetic field require more time to implement, either because the method is time consuming (flux-pumping, persistent mode switch), or simply due to the inherent coil inductance creating a time delay if using dedicated current supplies. The presence of the magnetic field also increases the path length of the travelling electron, as it is forced to move in a helical path of pitch dictated by the

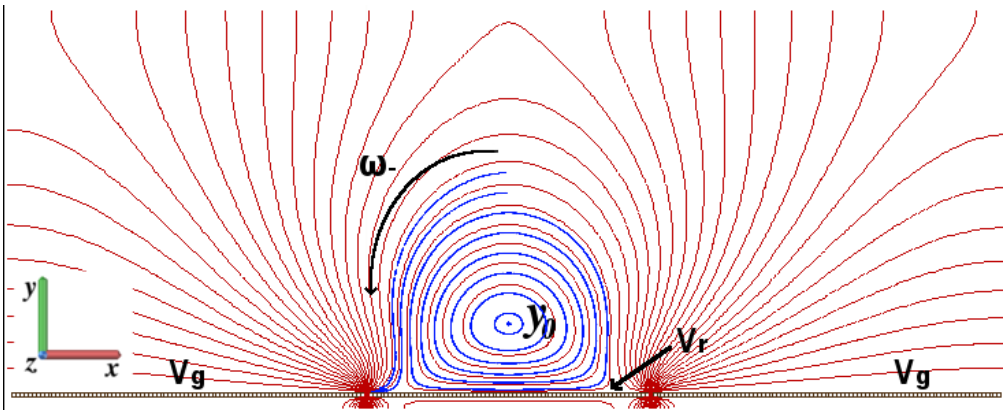


FIGURE 2.22: Shown is a SIMION simulation of electrons in the Geonium Chip trap. In this example, the electrons are generated with initial positions $(0, y_{\text{in}}, 0)$ with energy $E = k_{\text{b}}(4.2\text{K})$, where y_{in} takes a range of values from y_0 increasing in y_{in} until the particle is no longer contained. The particle paths are marked in blue, and it can be seen that they follow the curvature of the equipotentials [16, 17]. If the equipotential line forms a closed loop around the trapping region, then the particle is contained. Particles generated within closed potential loops are thus contained, whilst particles outside are lost to ground.

direction of initial ejection. This increases time of flight, and hence the probability of capture. Various scenarios intended to replicate these were simulated.

- **Constant Homogeneous Field** In the case of a constant homogeneous field, like those found in a large solenoid magnet, the loading was perhaps the most straightforward. Simulation results can be seen in figure 2.23. Beginning with 0V on all electrodes, the UV light is applied and a cloud of electrons will be generated, with energies of approximately 0.07eV at the illuminated wall. This corresponds to an electron ejected from a gold target by 240nm light (equation 4.1), and has an equivalent temperature of roughly 812K. The electrons are confined by the magnetic field to travel in tight helical paths centred around the magnetic field lines, and so it can be expected that a significant proportion of the electron cloud - those electrons generated at $(\ 0,\ y_0, -10\text{mm})$ will travel into the central region, i.e. the trapping volume. When the electrode voltages are applied simultaneously, any electrons travelling through the trapping volume will be caught, resulting in a cloud of trapped electrons. Note that the trapping volume is not the same as the useful trapping interval mentioned in section 2.2.1, and is much larger in size. It simply refers to the region where a particle will be confined, in other words the region of potential greater than the energy of the electrons. The loading sequence for this case will be:

1. Homogeneous $\vec{B}$ field is on from the start of the process.
2. Electrodes are set to 0V
3. UV light is applied to wall at z=-10mm, flooding region with electrons travelling parallel to trap surface.
4. Apply trapping voltages V_r, V_c, V_e
5. Particles are now trapped in trapping volume - apply cooling to observe in useful trapping region.

When initially trapped, the particle motion will have extremely large amplitudes because of the effective temperature, and hence the particle must undergo a number of cooling stages before it can be observed, as well as reducing the number of particles in the trap. The consequences of this mean that to initially load the trap in this case, the only requirement is that there is a non-zero number of electrons inside the trapping volume at the point of electrode switch-on. The magnetic field is already confining the particles in the x and y directions, and so all that remains is to add the axial confinement. The particles will initially have high energy, and large amplitudes of motion, however this is not a problem, as in any real trap they will rapidly cool through radiative processes, from which point the number of particles can be reduced and resistive and magnetron cooling can be applied to the particles to reduce the motions to within measurable limits.

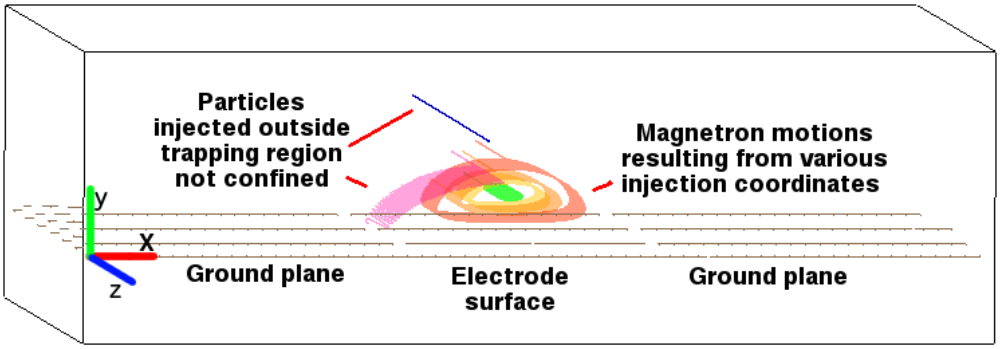


FIGURE 2.23: Particles were injected at the chip wall, with an energy of 0.07eV ±10% to replicate photoelectric expulsion by a 240nm photon. The entry coordinate on the wall, and entry cone angle were randomly varied. The homogeneous field makes the cone angle variable largely redundant, as the electron is confined to travel along the magnetic field line, and only served to modify the pitch of the helical path taken, not the mean direction of travel. The most important variable in the case is the entry position. It can be seen that any electron present in the trapping volume is confined, and held in an eccentric magnetron orbit corresponding to the equipotential line at point of entry. Particles outside the trapping volume (magenta, blue) are lost to ground.

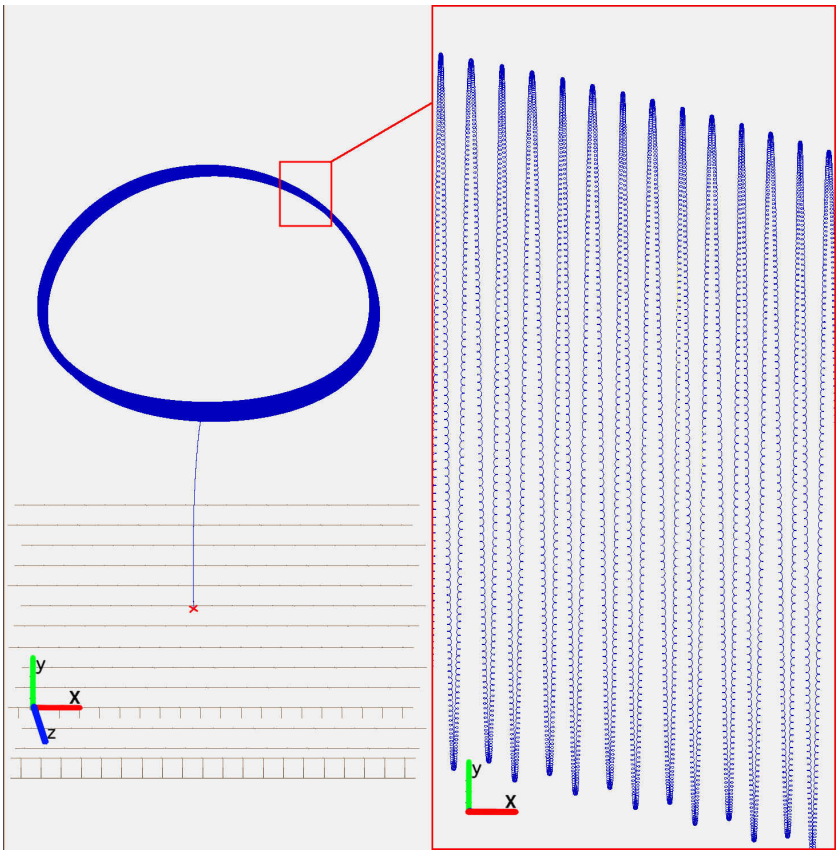
- **Switch-able Homogeneous Field** This case is almost identical to the constant case, with the exception that the electrons experience no magnetic deflection until the field is switched on. In the simulation, the field was switched on instantaneously, whereas in reality there is a rise-time associated with the coil inductance. In this case the loading sequence is:

  1. Homogeneous $\vec{B}$ field is off, B_z=0
  2. Electrodes are set to 0V
  3. UV light is applied to back wall and chip surface, flooding region with electrons travelling in random directions to ground.
  4. B_z and trapping voltages V_r, V_c, V_e applied simultaneously (If B_z applied first, then case reverts to constant field scenario)
  5. Particles are now trapped in trapping volume - apply cooling to observe in useful trapping region.

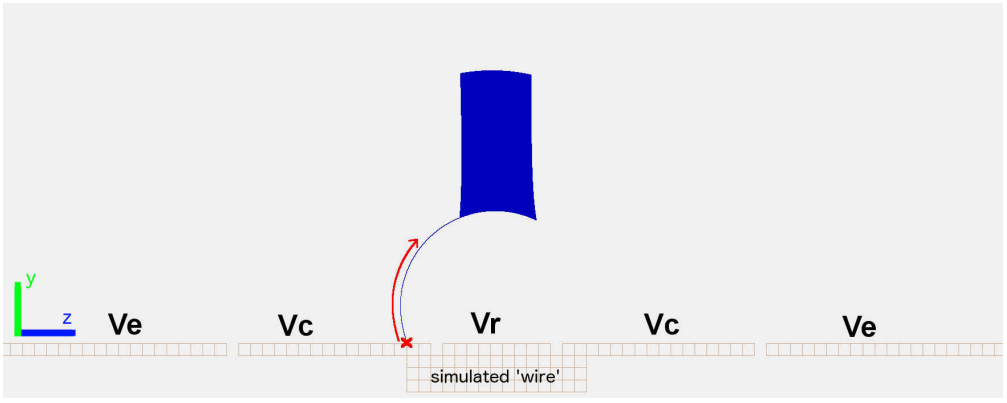
- **Magnetic Wires** To test the tendency of electrons to follow lines of field, magnetic sources were added to the simulation in place of a homogeneous field, in order

to mimic wires under the chip. *SIMION 8.0* has no way of easily representing magnetic fields in terms of currents and densities, instead the magnetics take the form of magnetic scalar potential arrays. So then, a wire of the same dimensions as the central wire of the prototype planar magnetic field source - discussed in section 2.4 with dimensions found in table 7.1 - was approximated, and it was seen that in this case loading was best performed by generating electrons from the surface of the electrodes. The approximately circular trajectory of the electron meant that only those electrons generated at a position $x \approx 0, z \approx \pm y_0$ will have a trajectory which leads to the trapping volume. A demonstration of trapping is seen in figure 2.24(a). As this is a single, un-compensated wire, the axial motion exhibits a large curvature and the resultant travel in the y direction is shown in figure 2.24(b). In this scenario the magnetic field is constant, as would be expected from a flux-pumped persistent-mode coil (see section 7.3.6 for details), and the electric fields switched from 0V to the trapping voltages when the electron reaches the trapping volume.

1. Simulated wire $\vec{B}$ field is on
2. Electrodes are set to 0V
3. UV light is applied to chip surface, flooding region with electrons travelling in arcs around the wire.
4. Trapping voltages V_r, V_c, V_e applied simultaneously
5. Particles are now trapped in trapping volume - apply magnetic field corrections and cooling to observe in useful trapping region.



(a)



(b)

FIGURE 2.24: Trapping from an approximated single wire is shown. The electrons are injected at the surface of the trap (point marked with a red cross) and can be seen to move in arcs centred on the axis of the wire, following the lines of field. Electrons with trajectories that take them through the trapping volume will be confined when the trapping voltages are activated.

Chapter 3

Design of the Geonium Chip

The Geonium Chip is motivated by the goal of trapping a cloud of electrons, and with future optimisation steps e.g. improved magnetic field stability and detection electronics, observing a single electron in a planar Penning trap - a goal not yet achieved by any group at time of writing. The chip is based on the design detailed in [12], and has a design different from other planar Penning traps in the way that the magnetic field points parallel to the electrode surface, allowing the axial potential to be symmetric - a problem which has thus far restricted precision in planar trap designs with the magnetic field normal to the surface [45, 76]. The direction of the magnetic field means that the Geonium Chip is an elliptical trap, but as discussed in section 2.2.3, this can be compensated for, and has no effect on measurement precision.

Initially it was intended to prototype the chip with fabrication techniques similar to those used in existing cylindrical Penning traps, with separate macro-scale electrodes insulated with sapphire (figure 3.1).

In the end, this macro-scale design was deemed too complicated to manufacture, and the manufacture cost and time would outweigh the benefits, so it was decided to have the chip made in a clean room.

Designed in close correspondence with *Mir Enterprises*, the chip design took many directions before the first generation chip was settled upon. Discounted designs include double sided chips, chips with through-wafer vias and chips with holes or notches for alignment and mounting. All were discounted for various reasons, including cost, lead-time of manufacture, and practicality. Any physical defect (such as a notch or hole)

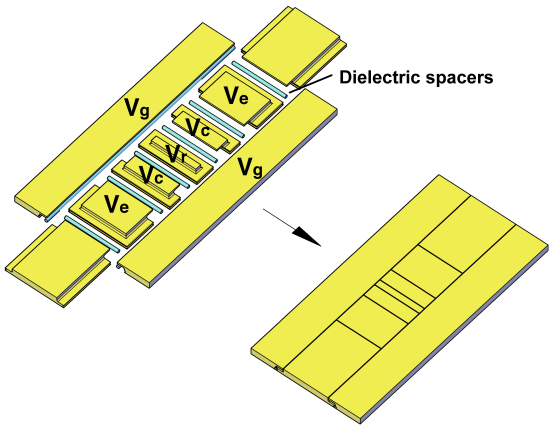
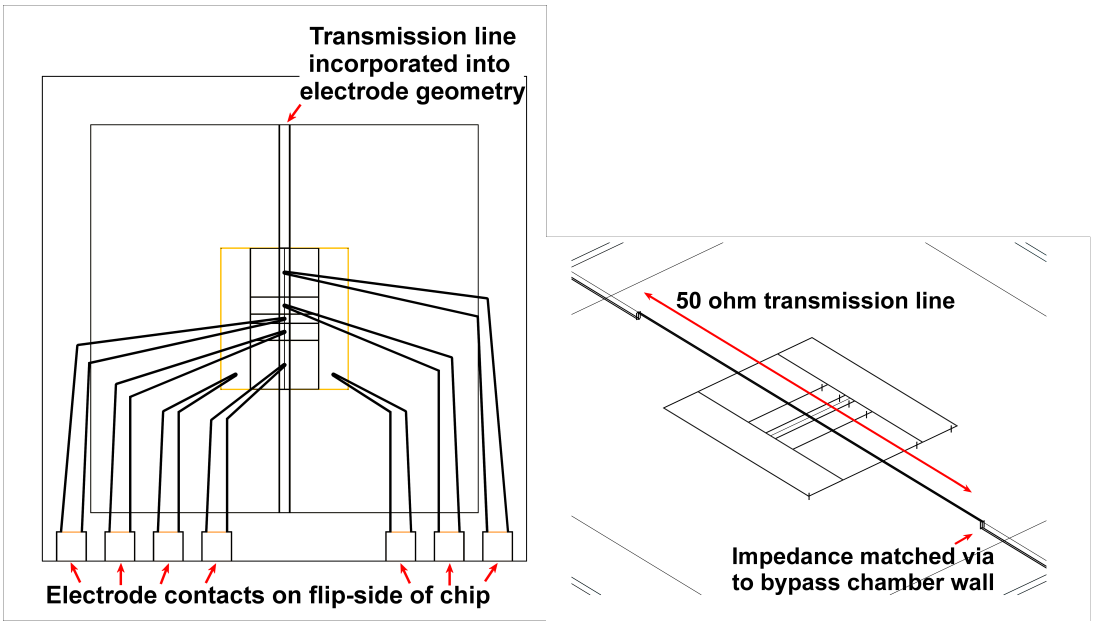


FIGURE 3.1: The earliest designs resembled the well-known cyclindrical Penning trap in construction.

to a crystalline substrate like silicon, would likely cause splitting, by allowing cracks to propagate and cleave along the crystal axis, making the chip physically weak and susceptible to breakage during handling and thermal cycling.



(a) (b)

(c) (d)

FIGURE 3.2: A selection of discarded designs for the Geonium Chip. All designs featured the same fundamental electrode layout, but with varying features and substrate geometries, for example centrally mounted CPW and vias 3.2(a), integrated CPW with through-chip microstrip-CPW transition 3.2(b), seperate chip and ground-plane, with CPW 3.2(c) and 3.2(d).

3.1 Microfabrication

The first generation design settled on a simple rectangular shape, of 60mm ×40mm in z, x respectively, able to fit 4 full chips on an industry standard 6-inch silicon wafer, in a simple to dice pattern. A freshly fabricated silicon wafer is shown in figure 3.3.

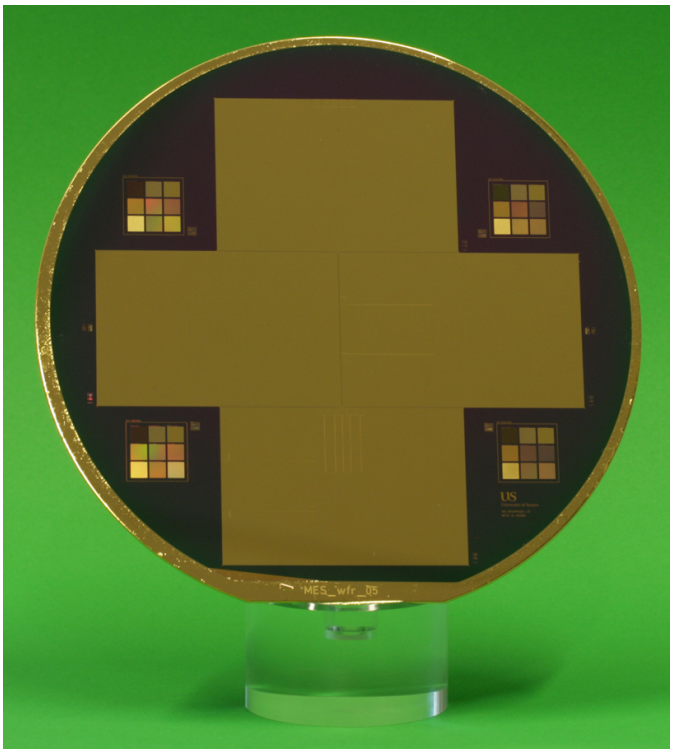


FIGURE 3.3: A standard 6-inch wafer carries 4 x Geonium Chips, shown in gold. The 10µm wide gaps between the electrodes are almost invisible at this scale.

The ideal Penning trap has no dielectric material visible from the point of view of the electron, as it can collect static charge to the degree that it distorts the electric potential from the electrodes, and it is difficult to purge the charges once accumulated. In other Penning traps, specialised geometries are employed which make use of overlapping conductors to minimise dielectric exposure, commonly employed in traps with rotationally symmetric electrodes. However in the Geonium Chip, the electrodes are not notationally symmetric, and there is no way to overlap electrodes such that 100% of dielectric is covered. It was decided to simplify construction and have a single layer of metallisation, and make the gaps between adjacent electrodes as small as possible.

This then posed the problem of voltage breakdown of the insulation between the electrodes, as any spark jumping the gap would cause unregulated current to flow and would damage the surface of the chip, rendering it useless for measurement purposes.

Aiming for a maximum applied voltage of 10V, this gives a start point from which to calculate the minimum electrode spacing required to avoid arcing and chip failure. It is clear from table 3.1 if the chip is used in air (as it would be for preliminary testing)

TABLE 3.1: Breakdown voltage of chip materials

E_{max} for chip materials in V per µm		
Air	Vacuum	Silicon Dioxide
3.0	220[77]	15-25 [78]

then the threshold for arcing is significantly lower than when in vacuum. It can be seen that for 10 volts, breakdown can be expected at the spacings listed in table 3.2.

TABLE 3.2: Breakdown distance for chip materials for a 10V potential difference

Breakdown distance for chip materials in µm		
Air	Vacuum	Silicon Dioxide
0.333	0.0046*	0.067 - 0.04

*included for consistency only, as other chip materials will break down well before the vacuum

To err on the side of caution, the chip was manufactured with an electrode spacing of 10µm. This would allow approximately 30 volts of difference between two electrodes in air, and upwards of 150V in a vacuum, before arcing could be expected. While 30 volts is significantly higher than the experiment should ever require, precautions must still be taken to avoid damage via electrostatic discharge, as an ESD can be many hundreds of volts.

3.2 Manufacturing Method

The fabrication of the Geonium Chip was performed in a clean room at *Mir Enterprises*. Several prototypes of the Geonium Chip were considered - a macro-scale flattened electrode stack of similar construction to existing cylindrical stack (see figure 3.1), or a printed-circuit board substrate with etched electrodes - but the decision was taken to move straight to microfabrication to obtain the maximum precision in the first generation chip.

3.2.1 Substrate Considerations

The substrate chosen for the chip manufacture was silicon, primarily because silicon is a well established material in semiconductor processing, with extensive research available to accurately reproduce designs. Silicon is not insulating, rather it is a semiconductor. The wafers used for the Geonium Chip are standard boron doped *p-type* silicon, with a room temperature resistivity of $17 - 23\Omega$cm and a crystal orientation of $\langle 100 \rangle$. It should be noted that at cryogenic temperature, the silicon experiences 'Freeze Out', where all the charge carriers previously in the conduction band drop to the lower energy valence band, and the material becomes non-conductive [79]. Various thicknesses of substrate were ordered in order to provide a degree of protection should one thickness prove unsuitable, for example if we had trouble with chips breaking under the stresses involved with mounting and thermal cycling, then a thicker wafer could be used. Two wafers of 675µm were ordered along with two of 800µm and one of 1000µm. Unfortunately the 800µm wafers had become scratched before arrival at the fabrication facility, shown in figure 3.4, and had to be substituted for two more 675µm wafers. It should be noted that in the absence of mechanical failure, a thinner substrate is preferable as it allows any parts mounted under the chip to be closer to the trapping position, such as the magnetic field source, or any coplanar waveguide lines used to communicate with the electron.

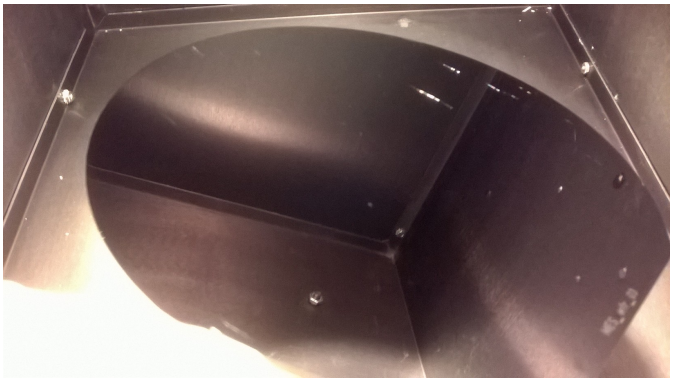


FIGURE 3.4: Damaged 800µm wafer discarded after an inspection revealed scratches on the wafer, visible in the top right hand corner

To insulate the electrodes and wires from the bulk Si, a layer of SiO_2 was first thermally grown onto the substrate to a thickness of 500nm. This would be the main substrate on which the chip layers were deposited. The electrical properties of the substrate are listed in table 3.3

TABLE 3.3: Electrical properties of the silicon substrate

	Properties		
Material	Resistivity Ωcm	Dielectric Constant ϵ_r	Loss Tangent $Tan\delta$
Silicon (300K)	17-23	11.9	> 1 [80]
Silicon (4K)	$\simeq 1 \times 10^{5}$* [79]	11.45* [79]	2×10^{-4} [79]
Silicon Dioxide	$\simeq 1 \times 10^{12}$ [81]	3.9	$\simeq 1 \times 10^{-5}$ [82]

* extrapolated from 10K data

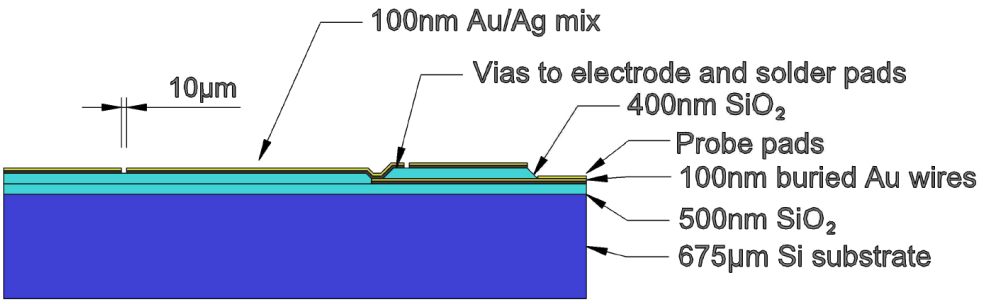


FIGURE 3.5: Sketch of the various layers of the Geonium Chip

3.2.2 Buried Wires

The choice to use buried wires stemmed from the desire to do-away with bulky vacuum feedthroughs in the cryogenic region, saving both space and cost. The buried wires take the form of microstrip lines, approximately $5 - 800$nm beneath the surface of the chip depending on the thickness of metallisation. The wires are electrically separated from the metallic ground-plane region by a distance $d = 400$nm SiO_2, and have a width W of 3µm, giving a width/separation ratio of $W/d = 7.5$. This was dictated by via fabrication methods, as ratios of less than this ran the risk of improper formation of the vias connecting the wires with the top surface. This unfortunately gives less than optimal high frequency performance. Using equations from [83], the characteristic impedance Z_0 of the line is worked out as

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_e}[\frac{W}{d} + 1.393 + 0.667 \cdot ln(\frac{W}{d} + 1.444)]} = 18.436\Omega \quad (\text{for } \frac{W}{d} \geq 1) \tag{3.1}$$

So as to limit disturbance to the top surface, the wire layer thickness was limited to 100nm, giving a cross sectional area of $0.3\mu m^2$. This limits the room-temperature capabilities of the chip, as the room temperature resistance is on the order of 1.7kΩ so high frequency measurements are subjected to significant attenuation.

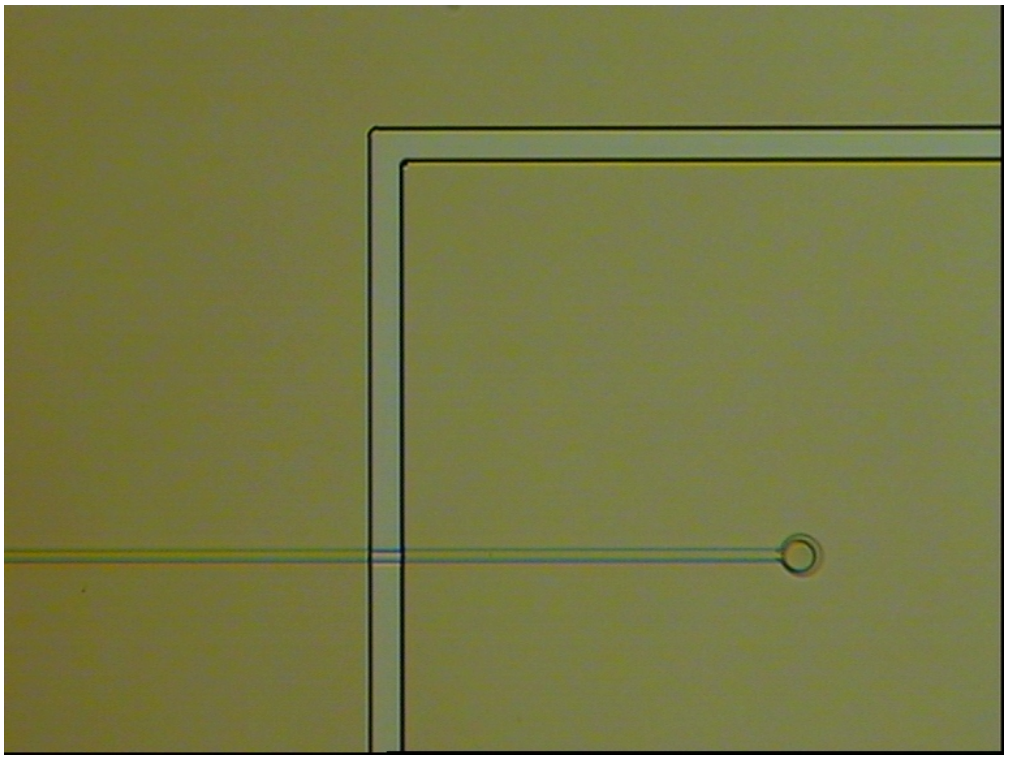


FIGURE 3.6: Here a microscope image taken at *Mir Enterprises* shows the 10µm separation between the electrode and ground plane, as well as the 3µm buried wire with via to the top layer.

3.3 Probe Card

The thickness of the metallic layer deposited on the chip presented a problem with regards to connecting to the chip electrically. The layers were so thin that conventional soldering methods would dissolve the contact pad [84], and were thus not possible. The layer was also too thin for standard wire-bond techniques, which required a minimum of 300nm or recommended 1µm metallisation [85, 86], whereas the Geonium Chip has metal contacts as thin as 100nm. One solution considered was to simply make the contact pads thicker. The downside of this is that an additional mask and manufacturing step would have to be incorporated into the fabrication stages. Another reason for not opting for this is that solder and wire bonds are semi-permanent solutions, requiring time and effort to make and break connections.

The option chosen was to use wafer probes to lightly contact the pads in a non-permanent way. Making the connections this way allowed for rapid connecting and disconnecting during initial tests, without damage to the contact pads. Acquired from *Accuprobe Inc.*, the wafer probes tips are made from a fine gauge Beryllium-Copper wire, 254µm in

diameter with a rounded tip, mounted onto a height adjustment system. Controlled with a fine brass screw, the height is adjustable ±0.635mm.

A fan shaped arrangement was chosen in order to access the contact pads without overcrowding the detection side of the probes, and to allow for the attachment of standard sizes of coaxial connectors and DC wiring. One downside of the wafer probes is that they are best suited to DC applications, as they are not designed with high frequencies in mind. Thus, they add some inductive and capacitive elements to the detection system which need to be measured in order to be properly accounted for. That said, any method of bonding to the chip would have some unwanted frequency dependent parasitic contributions, as these are nearly impossible to completely avoid.

3.3.1 High Frequency Analysis

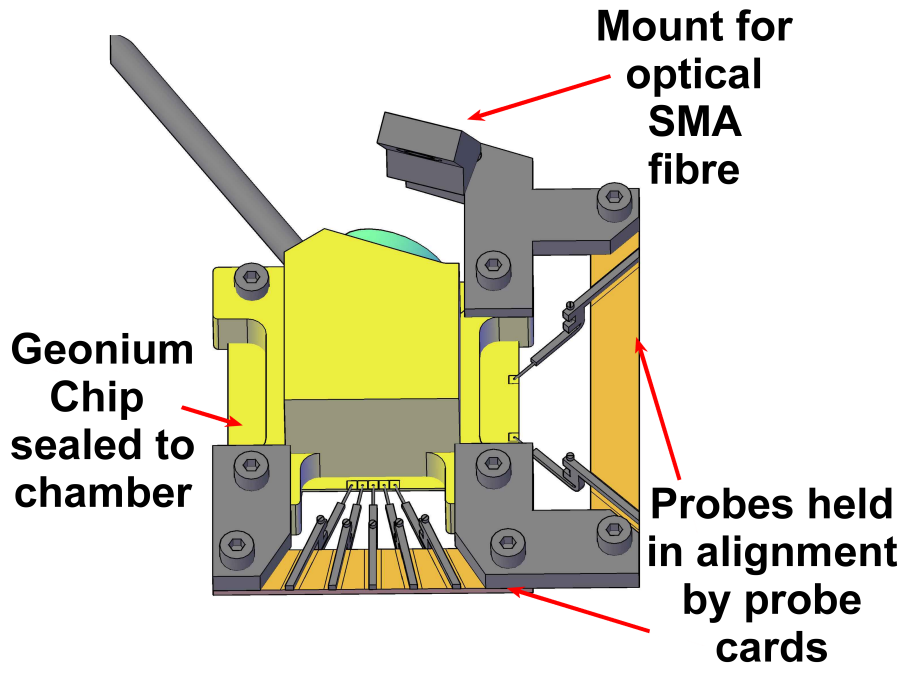
In order to measure the parasitic capacitance of the chip and probe card, the S-parameters (scattering parameters, equation 3.2) were measured with a *Keysight N9923A Fieldfox* vector network analyser (VNA). By connecting the chip as a series of two-port networks, figure 3.8, S-parameters were obtained for each of the possible connections. Of most interest are those parameters associated with the correction electrode, as this is the designated pickup electrode for the axial frequency ω_z.

In terms of voltage, the scattering parameters of a two-port network are defined as

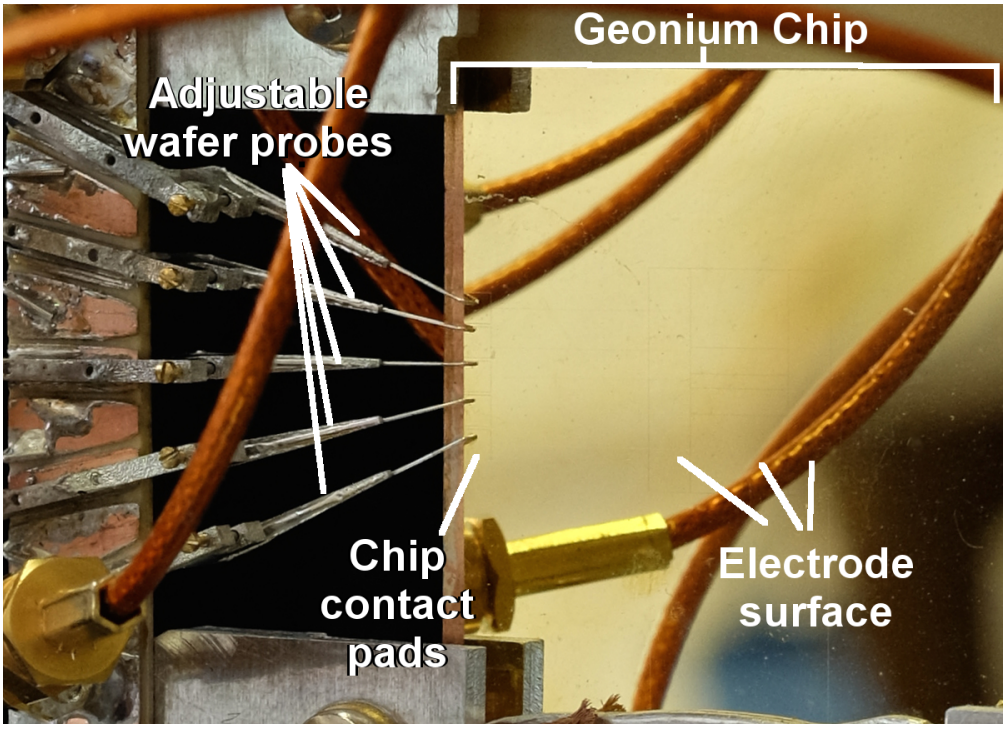
$$\begin{pmatrix} V_1^- \\ V_2^- \end{pmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{pmatrix} V_1^+ \\ V_2^+ \end{pmatrix} \tag{3.2}$$

where $V_{1,2}^+$ is the stimulus signal sent by ports 1 and 2 of the VNA, and $V_{1,2}^-$ is the voltage received by the ports i.e. the voltage reflected from the DUT.

Although the chip electrodes are all DC isolated, at higher frequencies, the electrodes are coupled together by parasitic capacitances. Each of these acts a 'real-capacitor' (figure 3.11(a)) with associated parasitic inductance, capacitance, and resistance. Considering the Geonium Chip as two-port networks gives a total of 21 possible networks, or 28 if the ground plane is also included as a port. A sketch of the network is shown in figure 3.9. As the signal path has contributions from all of the possible paths, the total effect of all the parasitic elements is contained in the S-parameters.



(a)



(b)

FIGURE 3.7: The probe card contacting with a Geonium Chip is shown. In 3.7(a) a drawing of the card and cryogenic chamber and the integration of probes and chamber can be seen in order to access the contact pads on the Geonium Chip. The fan-shaped arrangement of the probes can be seen in figure 3.7(b), along with the contact pads and electrodes of the chip.

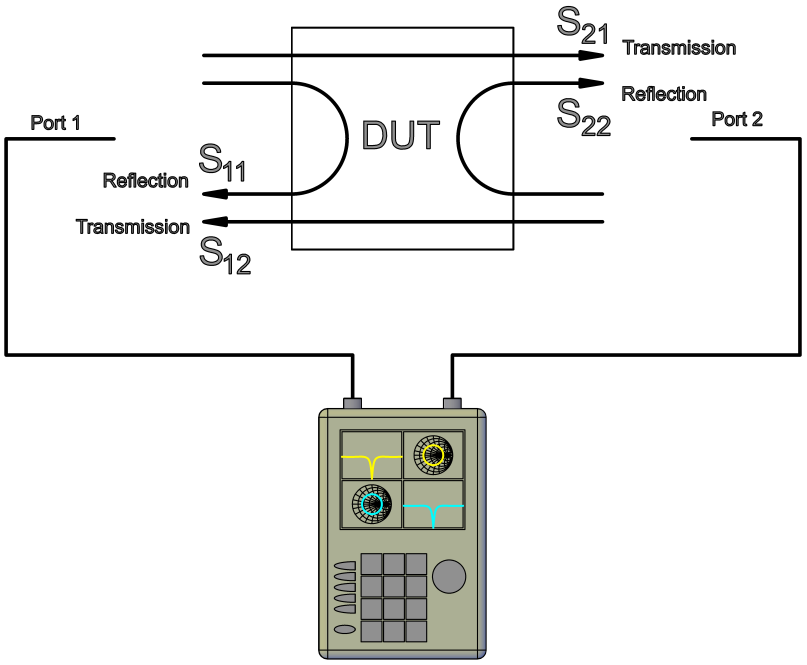


FIGURE 3.8: The VNA measures the transmission and reflection scattering parameters of a two-port network, as defined in equation 3.2.

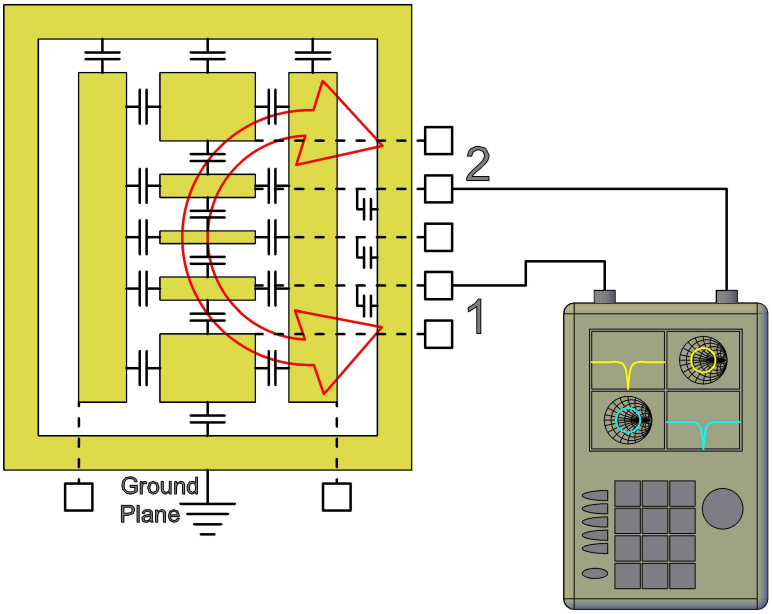


FIGURE 3.9: All the Geonium Chip electrodes are capacitively interlinked. Any of the possible two-port networks (correction to correction is shown for example) contain information about the total effect of the parasitic capacitances specific to that particular pair of ports, as the signal path includes contributions from all the possible paths through the network.

In order to determine the frequency dependent impedance of the probe-card and the buried wires, the values of R, C and L must be extracted from the S-parameters.

Any reciprocal two-port network (e.g. symmetric, passive networks such as the chip and probe card), can be expressed in terms of an equivalent π-network of admittances (Y-parameters) shown in figure 3.10. The Y parameter measurements contain all the information about the admittance at the input and the output of the two-port network. These can be any of the possible networks of the chip e.g. ring-correction, correction-ground-plane etc., and is measured from the reference plane of the VNA calibration (the reference plane in this case are the two ends of the coax cables), and thus also contains admittance information about the probe card. Transforming the S-parameters to give the Y-parameters using relations found in [83] gives the admittance matrix

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}. \tag{3.3}$$

In general, the elements of Y take form of complex numbers, with the imaginary component relating to the capacitance and inductance.

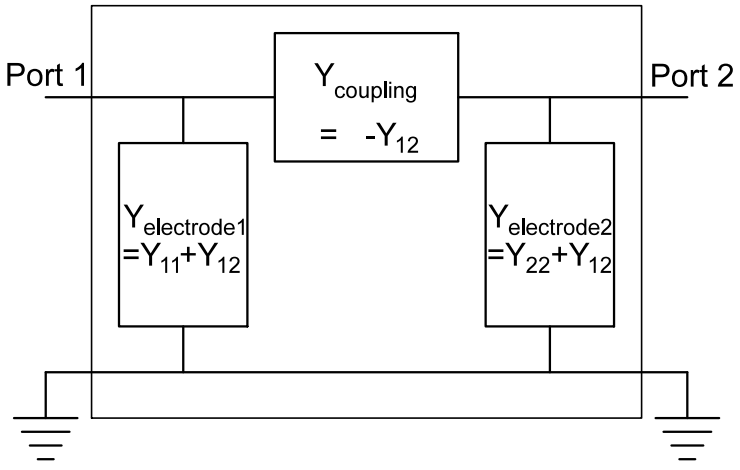
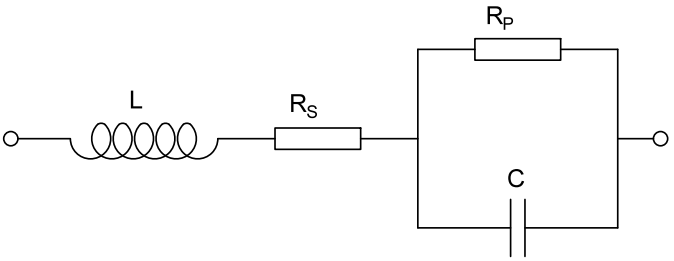


FIGURE 3.10: A reciprocal two-port network can be represented as a π-network of admittances.

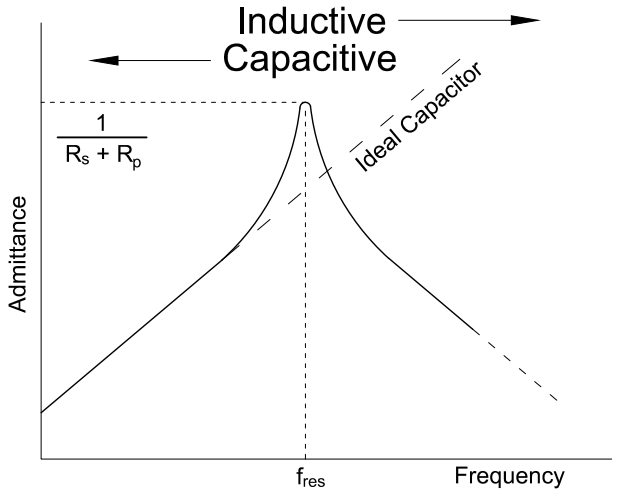
TABLE 3.4: 300K Geonium chip parameters. The three values for R_s, C and L relate to each of the three 'real capacitors' C_{re1}, C_{re2}, C_{re3} used in the fit model. (*The values in this table were acquired by A. Cridland of the Geonium group.*)

Electrode	$C_{re,n}$	Value ± Error		
		R_s (Ω)	L (nH)	C (pF)
Upper Endcap	C_{re1}	37.2 ± 0.2	44.3 ± 0.3	42.4 ± 0.4
	C_{re2}	63.7 ± 0.5	45.8 ± 0.5	1.11 ± 0.01
	C_{re3}	19.99 ± 0.07	25.8 ± 0.1	0.58 ± 0.003
Lower Endcap	C_{re1}	38.0 ± 0.1	34.9 ± 0.1	43.7 ± 0.3
	C_{re2}	79.8 ± 0.5	62.8 ± 0.6	0.882 ± 0.008
	C_{re3}	24.06 ± 0.07	21.92 ± 0.09	0.44 ± 0.002
Ring	C_{re1}	39.5 ± 0.1	51.3 ± 0.3	36.6 ± 0.3
	C_{re2}	75.7 ± 0.5	39.1 ± 0.7	0.841 ± 0.009
	C_{re3}	27.51 ± 0.08	28.7 ± 0.1	0.566 ± 0.002
Lower Correction	C_{re1}	38.3 ± 0.1	37.0 ± 0.1	43.0 ± 0.3
	C_{re2}	73.3 ± 0.3	54.1 ± 0.4	1.006 ± 0.007
	C_{re3}	26.3 ± 0.07	23.84 ± 0.09	0.448 ± 0.002
Upper Correction	C_{re1}	37.8 ± 0.1	42.0 ± 0.2	43.7 ± 0.3
	C_{re2}	61.0 ± 0.3	43.6 ± 0.4	1.195 ± 0.009
	C_{re2}	21.60 ± 0.06	2.4 ± 0.1	0.564 ± 0.002

By plotting the admittance measured and comparing to the 'real capacitor model' pictured in figure 3.11(b) [87], the chip was observed to behave as a parallel arrangement of 'real' capacitors, with distinct resonances. With a suitable model, the values of the reactive components could be extracted from a polynomial fit. As the first three peaks made the greatest contributions, the model used three 'real capacitors' in parallel, each with their own values of R_S, C and L shown in figure 3.11(a). Subsequent peaks were ignored as their contributions were so small the the resonances lay outside the region measured. R_P was fixed at $6.35 \times 10^{14}\Omega$ to reduce the number of fitting variables and allow the fit algorithm to converge on a realistic set of values. The table 3.4 details the extracted values over the range 2 to 1800MHz. It can be seen that the first capacitor is by far the largest contribution, and for the correction electrodes it is around 43pF. Adding this value in parallel with the detection coil detailed in section 6.5.1 will load the coil, and reduce the resonance down to the range of 20MHz. As the axial frequency is dictated by the trapping voltages applied to the electrodes, this frequency reduction is able to be compensated for.



(a)



(b)

FIGURE 3.11: Figure 3.11(a) shows the equivalent circuit of the 'real capacitor' model used to fit the chip response. It was found that the best fit was given by three 'real capacitors' in parallel. Figure 3.11(b) shows the frequency response of the admittance of such a circuit. f_{res} marks where the capacitor begins to self resonate, and the inductive effects take over as the frequency increases. Hence plotting Y gives a Lorentzian shape, which can be fitted to a graph to extract the parameters R, L, and C.

Chapter 4

Experimental Set Up

4.1 General Overview of the Vacuum System and Wiring

The experiment consists of two vacuum vessels. One is mounted directly on the Penning trap chip and is cryogenically cooled (detailed in 4.2,4.4), and the other much larger chamber encloses the whole set up to allow for the use of the cryogenic temperatures. The large external vacuum chamber that houses the experiment is spilt into two main parts. The largest part serves only to house the experiment, and provide a port through which to connect the vacuum pumping station (*Agilent Vacuum TPS Compact*), as well as support the whole experiment in its mountings. Sealed to this chamber with a $ISO200K$ flange is the smaller part of the chamber, which in addition to providing a mounting for the cold head, also contains all the flanges for the electronic wiring and fibre optic cables. The experimental set up itself is built around the cold-head of the pulse tube, which is sealed to the vacuum chamber with a diameter 140mm O-ring vacuum seal around the room temperature flange of the cold-head.

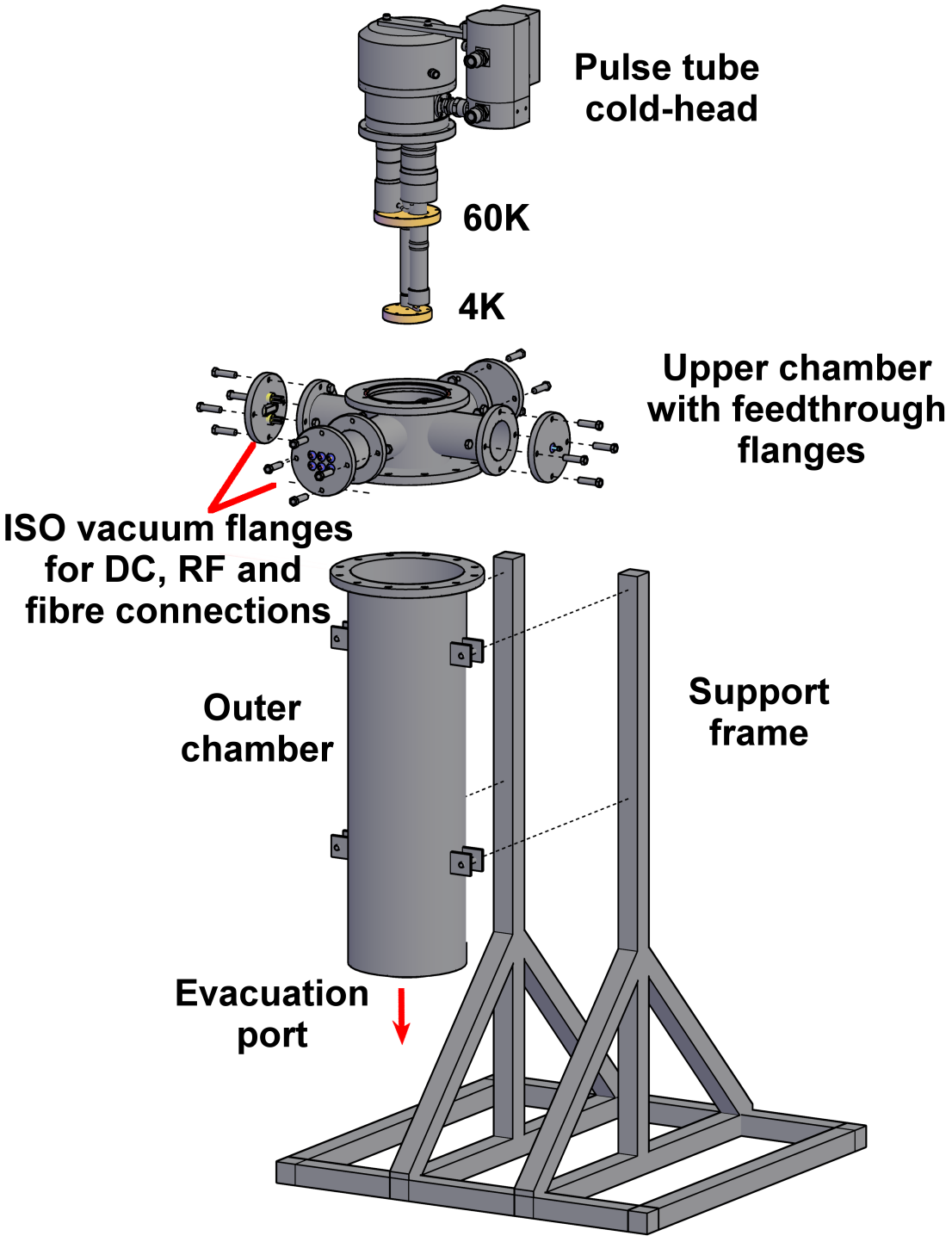


FIGURE 4.1: Exploded view of the two main chambers, feedthrough flanges and mountings. The top chamber and coldhead are removed together, with an electric hoist mounted on the ceiling.

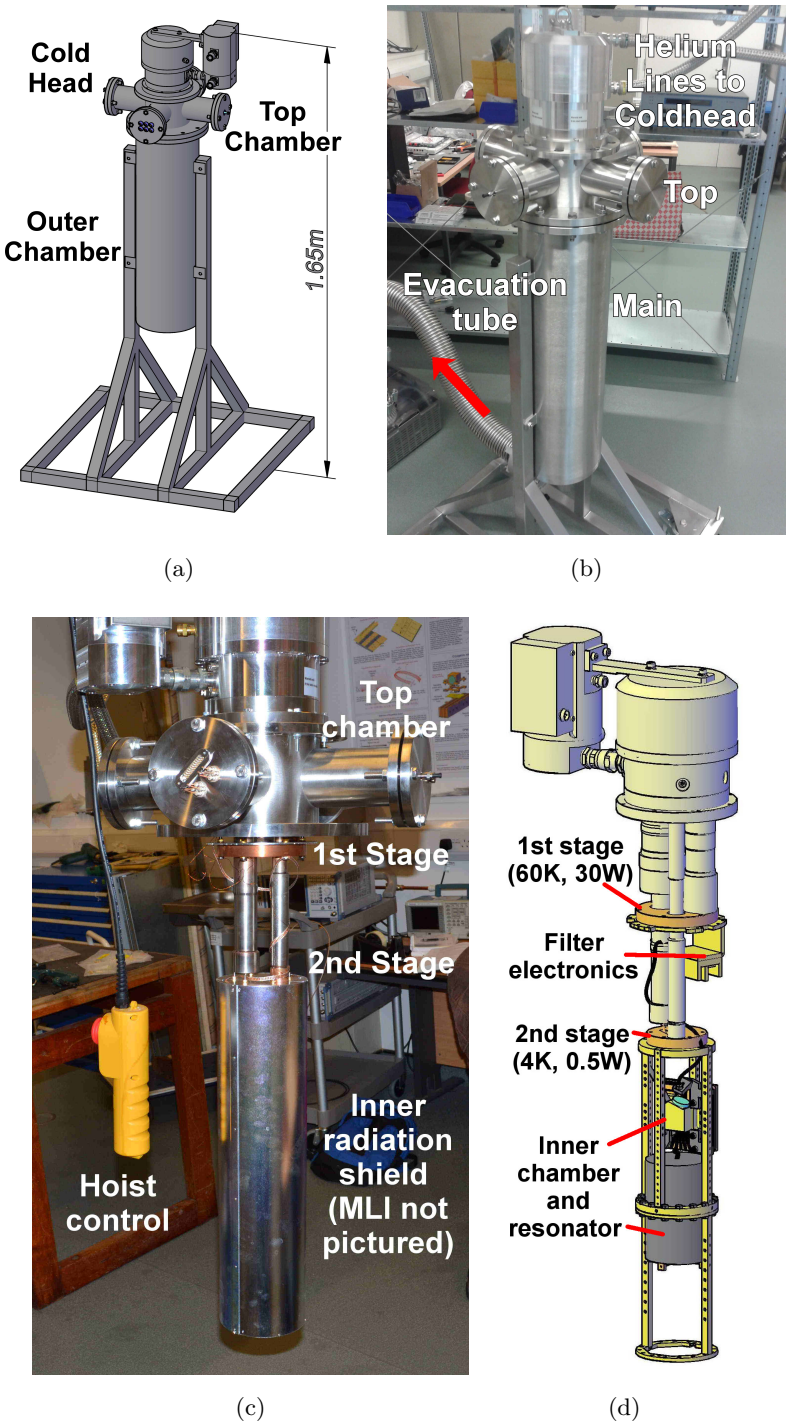


FIGURE 4.2: Figure 4.2(a) and 4.2(b) show the main vacuum chambers and the overall scale. Figure 4.2(c) shows the pulse tube and top vacuum chamber section, hanging from a central fulcrum point eyelet from a ceiling mounted hoist. The inner, 4K electro-polished aluminium radiation shield is seen enclosing the experimental area, without any multilayer insulation. In figure 4.2(d) a drawing of the inner components, Geonium Chip with cryogenic chamber, magnet coils and mountings and helical resonator.

The pulse tube has a two-stage cold head (*Sumitomo Heavy Industries SRP-062B*). The

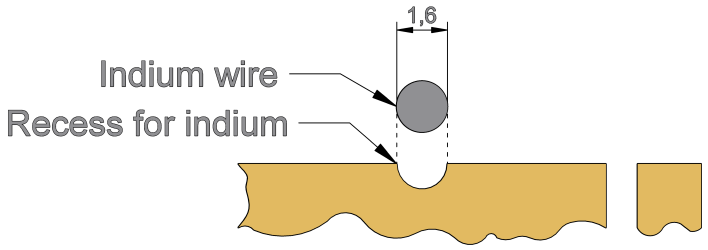
1^{st} of these stages is designed to have 30W cooling power at 65K, and the 2^{nd} stage to have 0.5W at 4.2K These were measured to be 60.1K (30W load) and 3.97K (0.5W load) in the Sumitomo Test Report.

The 1^{st} and 2^{nd} stage temperatures were monitored using Cernox resistor type temperature sensors (*LakeShore CX-1010-SD-HT-1.4L-P*).

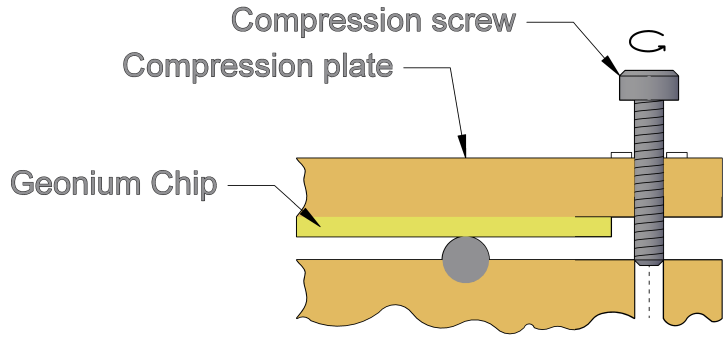
After the wiring is fed into the main vacuum chamber, in order to reach the first cooling stage, the wiring passes through the first electro-polished aluminium thermal radiation shield and MLI, where it is thermalised to approximately 65K. To reduce thermal and electromagnetic noise from external sources, the lines pass through a set of filters consisting of RC low-pass filters for the trap DC voltages (one at each thermalisation stage, each with a $f_{\text{cut-off}} \simeq 16\text{kHz}$), and thermally anchored attenuators for the coaxial lines attenuating between -1dB and -20dB to ensure that the central conductor of the coax is in thermal contact with the thermal bath.

4.2 General Overview of the Cryomechanical Set Up

In order to ensure maximum lifetime of the trapped particle, it is desirable to have the best possible level of vacuum. To achieve this, it was decided to use a method of enclosing the trapping volume within a smaller vacuum chamber and cooling this chamber down to cryogenic temperatures, a technique previously used to achieve extremely long particle lifetimes [88]. This chamber is first evacuated through a thin aluminium tube (⌀6mm) to a pressure on the order of $\sim 5 \times 10^{-8}$mbar, and sealed shut via pinch-off device. This pinch-off device uses mechanical pressure to cold-weld the walls of the aluminium evacuation tube to itself, sealing the chamber. A demonstration is shown in figure 4.4. All other seals on the chamber are made by compressing gaskets made from 99.99% indium wire to form cryo-compatible metal seals, shown in figure 4.3.



(a)



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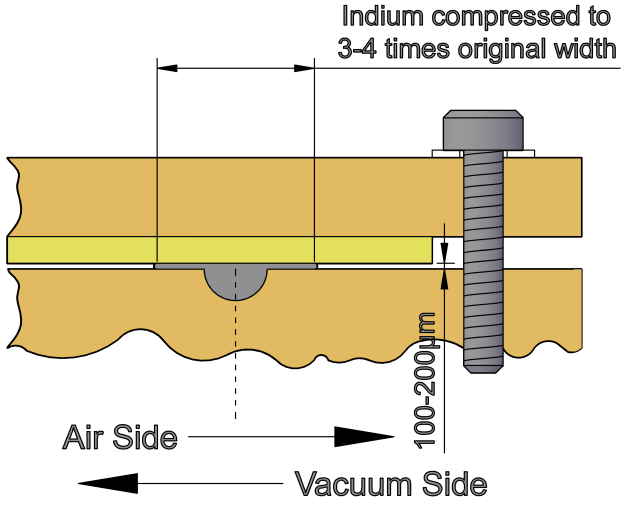
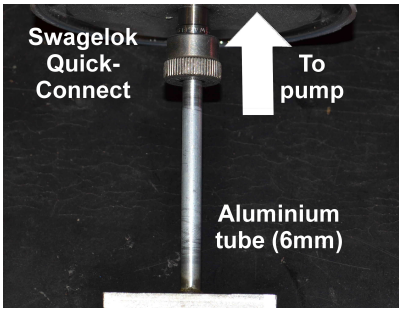


(c)

FIGURE 4.3: Sketch of indium compression to seal the Geonium Chip to the cryogenic chamber. In 4.3(a) the wire is laid into the groove, and the chip with the supporting pressure plate is applied in 4.3(b). During compression, the fresh indium is exposed as the wire deforms as shown in 4.3(c), and forms a cold-weld with the surfaces.



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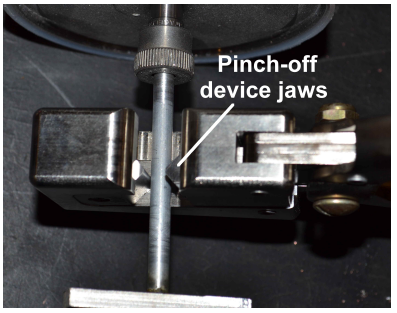

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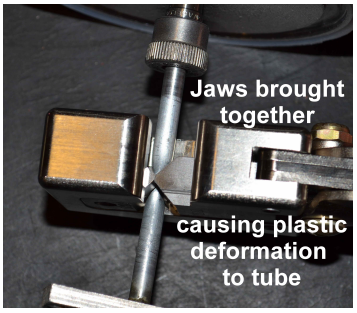

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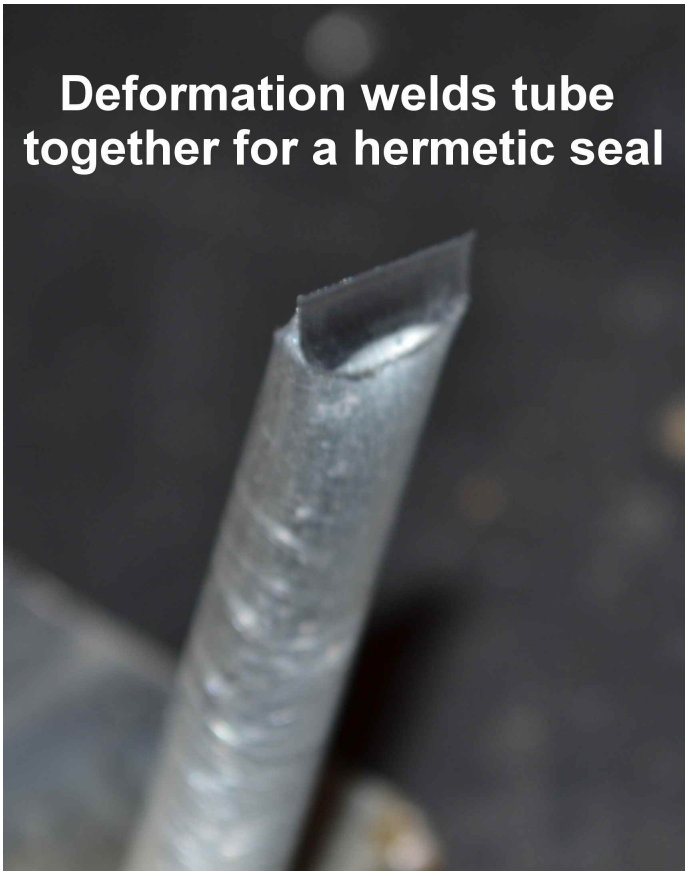


(d)

FIGURE 4.4: The operation of the pinch-off device is shown. Figure 4.4(a) shows the 6mm OD aluminium tube used to evacuate the cryogenic chamber. Also pictured is the *Swagelok Quick Connect* adapter to facilitate connection to the vacuum pump. The adapter is nominally designed for 1/8 inch (6.35mm) tube, but the seal tolerance is such that 6.0mm is perfectly acceptable also. Figure 4.4(b) shows the jaws of the pinch-off device (*CHA Industries - POD 375*[18]), able to accept soft metal tubes of up to 3/8 inch (9.525mm) with an outer wall thickness of 0.049 inches (1.24mm). In figure 4.4(c) the jaws are closed, and thus the weld is made. A close up of the pinched tube is shown in 4.4(d). The plastic deformation of the metal (and hence the cold-weld seam) can be clearly seen.

4.3 Heat Load Within the System

Opting for a 'dry' system rather than a liquid helium system offered advantages including increased portability, and low running costs - there is no need to continually top the system up with cold helium. The compressors and cold head are also designed for continual use, and so once set up, the system can be kept cold for many thousands of hours at comparatively little cost.

However it is not without its disadvantages, the main being the issue of heat load upon the system, and the final temperature is limited by the cooling power of the 2^{nd} stage, in this experiment this was 500mW. The final temperature is also not fixed, and can vary with heat load. A minimally loaded system could have a base temperature of below 2.5K. Great care must be taken to thermalise all wires linking parts of the system with different temperatures. In order to adequately sink the heat load into the cold head before it reaches the experimental region, the following points must be considered:

- **Clean Surfaces** - The contacting materials must be as clean as possible, with no oxidation or corrosion.
- **Maximum Contact Surface Area** - Heat flow scales linearly with surface area. Therefore, maximum thermalisation is achieved when the surfaces in contact are as large as possible.
- **Maximum Heat-pipe Cross-sectional Area** - Similar to above, but with the amendment that the heat must be sunk into the cold-head as quickly as possible once it has crossed the boundary. This is done by ensuring the lower temperature material has enough cross sectional area to adequately carry the heat away, or there is a risk of significant temperature gradients arising.
- **Clamping pressure** - If applicable, the two pieces should be held together as tightly as possible. This is primarily to ensure that maximal surface area is in contact, and hence contact conduction is improved.
- **Void Removal** - No two surfaces will ever mate perfectly, thus it is advised to use some fluid compound to fill any gaps left. A recommended compound is the *Apezion N* vacuum grease, as it maintains thermal contact at cryogenic temperatures, unlike other vacuum compatible greases which become brittle. As the heat

will have to flow through the compound, which is not a good conductor compared to metallic pieces, it is advised to use only a very thin layer to lightly grease the contact region.

4.3.1 Radiative Heating

To ensure infra-red radiative heating from outside the cold region is minimised, it was necessary to employ radiation shielding which completely enclosed the cooled volume. Initially, these were simply sheets of high-purity aluminium formed into cylinders and cut to make a tight fit on each stage of the cold-head.

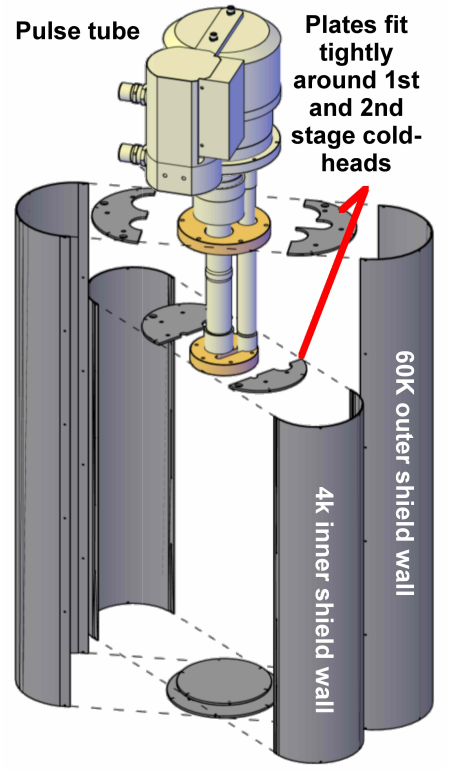


FIGURE 4.5: Exploded view of the basic radiation shield assembly, without any superinsulation. The larger of the shields encloses the 1^{st} cooling stage and is held below 60K, with actual temperature dependent on heat load. It also encloses the entire 2^{nd} stage, including its radiation shield and everything inside. The smaller shield is held below 4.2K and encloses the main parts of the experiment such as the helical resonator, low-temperature superconductor coils and the Geonium Chip itself, along with its cryogenic vacuum chamber. The top plates of the shields are split to allow a snug fit around the helium tubes which run up from the cold plates.

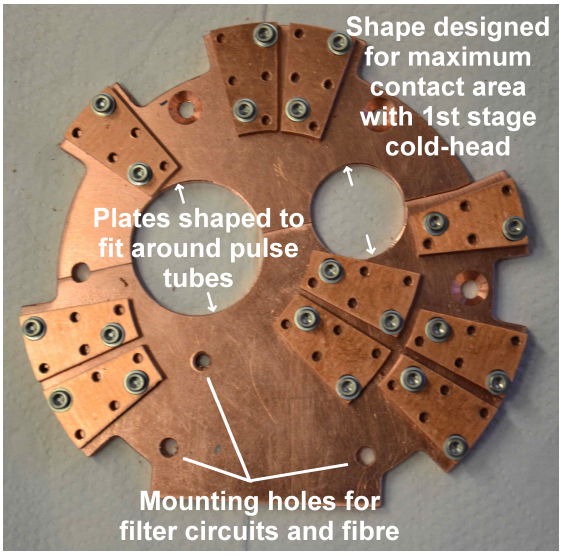
These were mechanically polished to a high finish and then electro-polished, in order to minimise emissivity. The inner (4K) cylinder has an internal diameter of 124mm, and a usable height of 480mm, forming the main working volume for the experiment. After

experiencing some heat load problems which resulted in the pulse tube not reaching the desired temperature of < 4K it was decided that a single aluminium layer provided inadequate shielding for our system, as the temperatures indicated that *tens* of watts were being transmitted to the 1^{st} cooling stage, which in turn presented a significant load to the 2^{nd} (the capacity map of the pulse tube is given in the appendix section A.1). A simple remedy was found in the form of multi-layer insulation (MLI), otherwise known as *superinsulation*, which is comprised of ten or more sheets of aluminized mylar, separated by low thermally conductive layers, obtained from *Scientific Magnetics*. This MLI was wrapped around all faces of the existing shields, as well as around the individual tubes of the cold head.

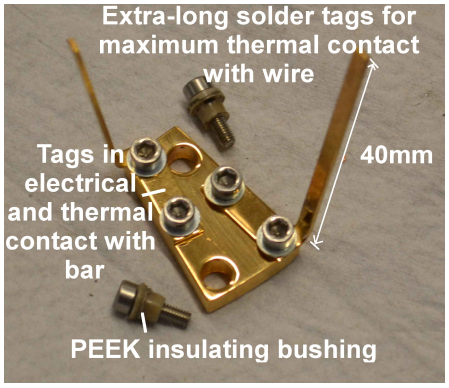
4.3.2 Thermal Wire Transport

The wiring between the system and the room temperature environment of the lab is a significant source of thermal load. In absence of currents, a copper wire on the order of a millimetre can raise the temperature at the experiment by several kelvin if it is improperly thermally anchored, and the heat is not sunk into the pulse tube. Heat flow tends to stay within a wire, and resists crossing boundaries between materials [69]. In order to ensure heat is properly sunk into the cold head, best practice is to have a physical break in the wire, with any current flowing through a bus-bar in thermal equilibrium with the cold head (figure 4.6(c)). In the Geonium Chip set up, these bus bars were electrically isolated from the bulk by mylar tape, and held tightly to the faceplate by screws electrically separate from the bus-bar. These can be seen in figure 4.6(b). The bus-bars are made to maximise surface contact with the coldhead faceplate (shown in figure 4.6(a)), with 4.2cm^2 of contact area. These were milled from OFHC copper, polished and gold-plated to prevent corrosion.

For the comparatively large currents needed for the magnetic coils, up to 8 thick (0.8mm optimised diameter) [89]. copper wires would be required to transport the currents between the 1^{st} and 2^{nd} stages. The thermal load well exceeded the cooling capability of the cold head, and the system struggled to reach temperatures lower than 6.5K, when testing with just two wires. The solution was found in the form of high-temperature superconducting tape, combined with the improved thermalisation blocks shown in figure 4.6. The 2mm HTS tape (further detailed in section 7.3.4), is composed of a stack of



(a)



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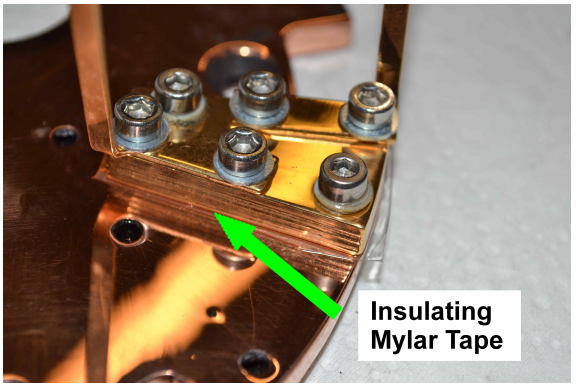


(c)

FIGURE 4.6: The faceplate is shown after machining in figure 4.6(a). In this image the bus-bar layout is being tested before it is polished and gold plated. Figure 4.6(b) shows the thermalisation bus-bar after gold plating. also shown are the mounting screws with PEEK plastic bushings to prevent electrical contact with the bar. The block is shown attached to the pulse-tube first stage faceplate in figure 4.6(c), isolated from the bulk by a sheet of mylar tape.

conductive layers, including two 20µm thick layers of electrical copper. The majority of the strip is composed of Hastelloy-C, which has a thermal conductivity of just over 2% that of copper at room temperature, and so is of little concern in terms of heat transport. Using this wire reduces the cross section of the wires to 0.08mm^2, just 16% of the 0.5mm^2 for each 0.8mm copper wire. This coupled with the complete elimination of ohmic loss in the wire greatly reduces thermal load, and means that there is now no 'optimal diameter' , adding flexibility to the values of current able to be used in the system.

4.3.3 Ohmic Dissipation

Ohmic dissipation is of concern only where large currents are involved, that is to say, currents larger than a few tens of milliamperes. Most of the electronic system has very little current requirement. However the magnetic field prototype requires relatively high currents. The system was intended to handle a maximum of 10A per wire, so there is potential for problematic ohmic heating if not properly addressed. Just 5mΩ is enough to exceed the cooling power of the second-stage coldhead at 10A. To combat ohmic losses, superconductors are used where possible. For the planar coils and second stage connections, low temperature NbTi superconductors were used, and between the first and second stages, 2mm width HTS tape was used to ensure ohmic in-wire losses were eradicated. This left the primary source of ohmic heat as the jointing between the superconductors, as we were unable to find a lossless method of joining two different superconductors. The best course of action is to maximise surface area in contact between the two conductors, as the resistance of any given conductor scales inversely with the surface area through which the current flows, and hence the dissipation also scales inversely with surface area. Surface area is also key for proper thermalisation, as thermal transport also scales with surface area. Thermal conductivity κ and electrical conductivity σ are related through the Wiedemann-Franz Law: $\frac{\kappa}{\sigma} = LT$, where L is the Lorenz Number $L = 2.44\text{W}\Omega\text{K}^{-2}$ [90], and for a given temperature T, both depend on many of the same factors. It would seem then, that maximising surface area and cross sectional area of current carrying parts is key to reducing ohmic dissipation. Unfortunately this approach falls down in cryogenic applications as the temperature difference is so great between components in the cryostat that the thermal transport down wires addressed in section 4.3.2 rapidly outweighs ohmic losses [89].

4.3.4 Component Considerations

The pulse tube cooling power also limits the power consumption of any devices at this stage, and restricts current flowing e.g. amplifier idle currents, as these also can cause heating through ohmic losses. Devices such as the amplifier board are expected to give out a certain amount of heat when in operation [91, 92], and must therefore be thoroughly thermally anchored to the bulk to ensure that the temperature is evenly distributed, with no hot-spots. This is particularly crucial as the temperature of the amplifier circuit

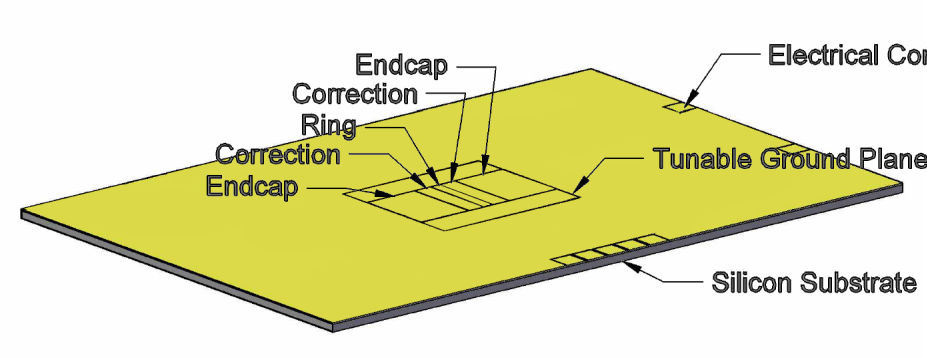
dictates the Johnson noise of the system, and as the system is in equilibrium with the electron, excess thermal noise can drive the electron to a higher temperature. Any thermal noise added to the signal will be amplified further as the amplification chain progresses, and the effect is greatest at this stage because the signal-to-noise ratio is the poorest.

The low temperature adds complications when designing the electronics, as component values change with temperature [7], and this must be taken into account when testing at room temperature. In particular, most silicon-based transistors exhibit 'freeze-out' below approximately 20K [93], so materials not susceptible to this phenomenon must be used. For the ω_z signal we chose gallium-arsenide transistors as the technology is well understood, and it has good noise characteristics in the frequency range required [94]. The detection circuits are discussed further in chapter 6.

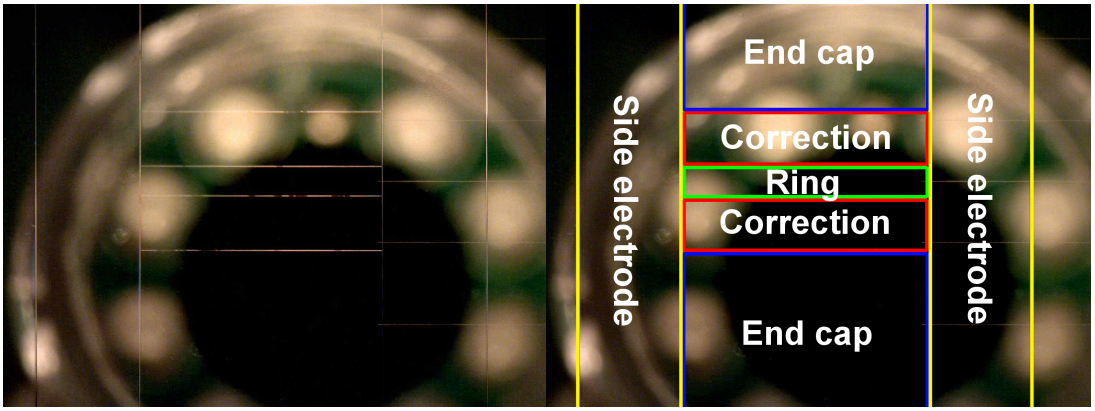
4.4 The Geonium Chip with Cryogenic On-Chip Vacuum Chamber

Bonding the cryogenic vacuum chamber directly to the chip [95] offers a number of key advantages. Firstly, the need for cryogenic compatible vacuum feedthrough connections is eliminated, representing a saving of both cost and space. The role of feedthrough is played by the buried wires microfabricated into the chip structure itself (figure 3.6), as the chip connection pads are brought outside the inner vacuum region. The chamber is directly bonded to the trap plane, so it is then simple to design the chamber with the correct shape and dimensions that it doubles as an off-resonant MW cavity, used to suppress spontaneous emission of the electron [96]. To have the greatest control over the magnetic fields in the trapping region and minimise the required current densities needed to generate the trapping field it is desirable to have our magnetic field source as close to the underside of the electrodes as possible. This is also desirable for any near-field microwave devices or waveguides passing under the chip. With the design we have chosen, this proximity is limited only by the thickness of the silicon wafer itself, around 675µm. This thickness is enough to hold a pressure difference of one atmosphere for a rectangular window of the dimensions of our chamber [97]. This only needs to be maintained for the preliminary evacuation before the inner chamber is placed in the cryostat. The seal is made directly around the active region of the chip, such that the

vacuum chamber forms a 20mm cube with the cube base consisting of the chip electrodes. One face of the cube consists of a metallic mesh screen detailed in figure 4.10.



(a)



(b) (c)

FIGURE 4.7: Figure 4.7(b) shows a microscope image of the electrode layout seen from the top (the reflection of the microscope can be seen in the surface of the chip). Figure 4.7(c) has the 10µm electrode boundaries highlighted with the 'ring' electrode in green, 'compensation' electrodes in red, 'endcaps' in blue, and tunable ground planes in yellow, as detailed in figure 4.7(a). The paths of the buried wires are visible travelling horizontally in the right hand side of 4.7(b) and 4.7(c).

It can be expected that the aluminium of the chamber will contract approximately 250µm between room temperature and 4K [98, 99], while the silicon is expected to contract much less, only around 13µm. Tightly confining a fragile piece of silicon such as our chip with epoxy or similar would lead to chip breakage, so the chip alignment recess takes these into account with a 500µm tolerance in the xy plane. Thus the chip is primarily constrained by the indium seal between the chamber and its surface. Indium is known to retain good ductility, even at cryogenic temperatures (hence its popularity for cryogenic seals), so any strains generated by thermal effects will be alleviated by the indium sliding between the two media.

TABLE 4.1: Expected thermal contractions upon cooldown

	$\Delta l/l$ (%)	Δl on a 60mm length
Aluminium	-0.415 [89]	250.8µm
Silicon	-0.022 [89]	13.2µm
	$\Delta r/r$(%)	Δr for a 25.4mm disc
Quartz	-0.15	19µm

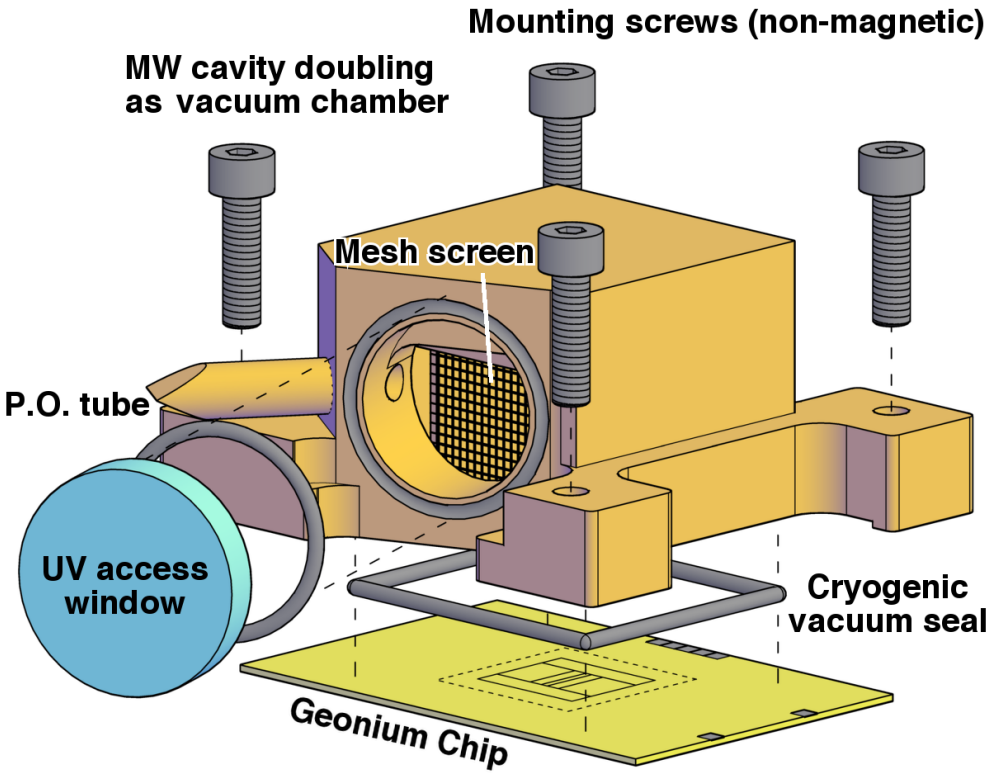
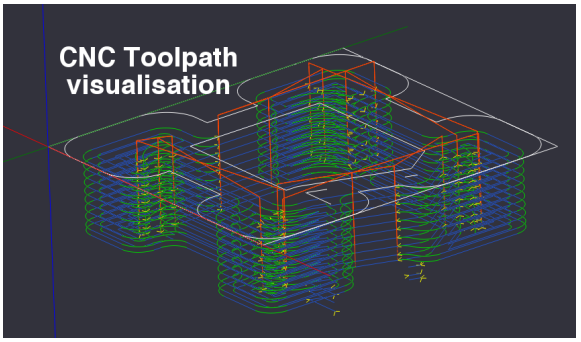


FIGURE 4.8: Shown here is an exploded model of the chamber. The indium vacuum seal can be seen between the chip and the chamber, to form the inner cryogenic vacuum.

It was decided to fabricate the chamber in house on a tabletop CNC router, partly to demonstrate the simplicity of our design, but additionally to add flexibility during prototyping. It also provided significant time and cost savings compared to external manufacture. A few materials were considered to construct the chamber. Out of the common choices for vacuum and cryogenic applications - copper, stainless steel, and aluminium, it was chosen to mill the main bulk of the chamber from a single block of aluminium, chosen for its ease of machinability and light weight, while also having good electric and thermal conductivity. Stainless steel was ruled out as a potential chamber material because of its ferromagnetic properties (even 'non-magnetic' austentitic stainless steels such as the 3xx series of alloys still have a comparatively large permeability).

Oxygen-free high conductivity copper was ruled out, as it involves more complicated machining processes. An overview of the machining process can be seen in figure 4.9



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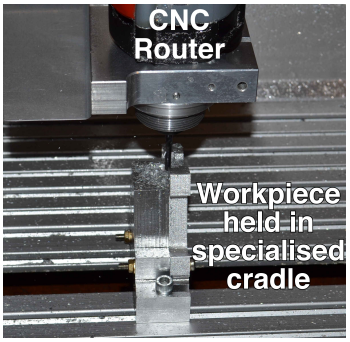

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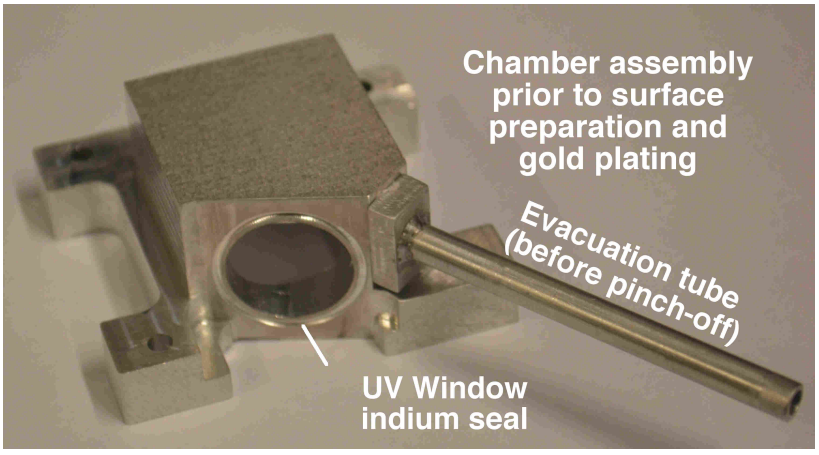

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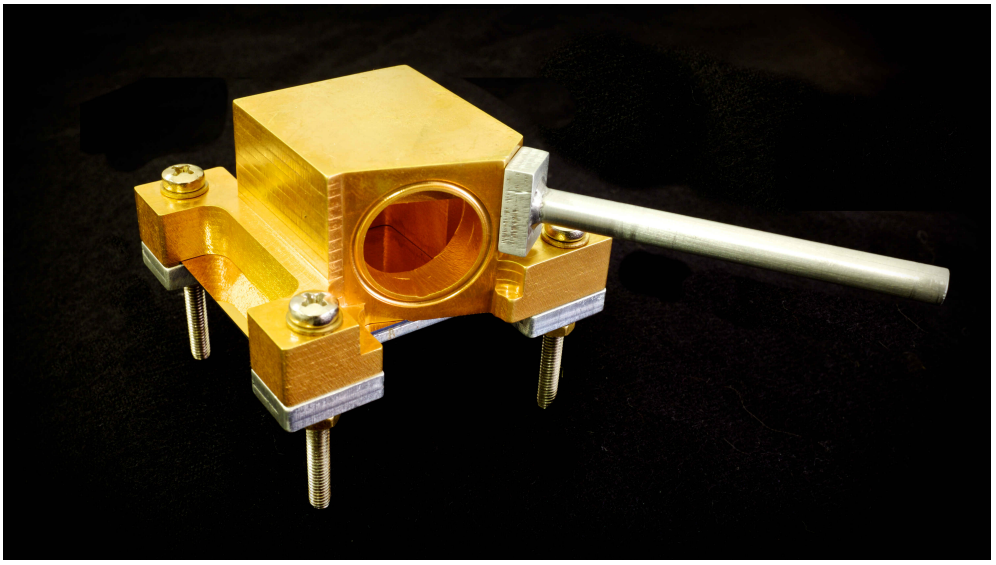


(d)

FIGURE 4.9: Various stages of chamber construction are shown here. Figure 4.9(a) shows a generated tool path used to generate the machine code necessary to control the CNC router. Figure 4.9(b) shows the chamber window in the process of manufacture, and figure 4.9(c) shows the milled chamber before gold plating, and after 4.9(d).

Although there are no laser optics in an electron only system, the photoelectric loading procedure still required optical access to the chamber. For this reason a fused-quartz window was included as part of the cryogenic vacuum chamber. To address the difference in thermal expansion coefficient between aluminium and quartz, the window is sealed with an indium gasket, the same method by which the chip is sealed. The low-temperature ductility of indium allows the window seal to deform without overly stressing the quartz. The inclusion of the quartz window presents a dielectric surface which needs to be screened from the trapping region. This was achieved simply by constructing one face of the MW chamber from a fine copper mesh with a hole size of 234×234µm, and a wire width of 19.8µm leaving an open area of 85%, obtained from *SPI Supplies*, in order to allow UV and visible optical access, while remaining reflective to the longer wavelength microwave frequencies. The mesh is mounted with solder in a $20 \times 26 \times 3$mm OFHC copper frame, with a frame thickness of 2mm, with the meshed open area of 16×22mm. This was then gold plated with a thickness of approximately 1µm. The mesh and frame are shown in 4.10. This frame is then held in electrical contact with the bulk of the chamber at the edges of the window. This allows the shorter wavelengths such as visible and UV to pass through, while shielding microwave and radio frequencies. The window is designed to slide into a slot in the base of the cryogenic chamber such that the mesh is flush against the face of the MW screening volume.

4.5 Precision Voltage Sources

Penning traps require ultra stable electric fields, as the stability of the field translates directly to measurement accuracy. Any noise in the electric field is transferred to the whole system including the trapped electron, broadening the detection signal and decreasing precision. For this first generation experiment, we required a certain flexibility and tunability in our design, hence we chose to use precision voltage calibrators (*Time Electronics*), which have 1µV adjustability and a voltage range of 0-22V, rather than fixed voltage supplies. To reduce external noise the DC lines are passed to the experiment via shielded coaxial cable, into an initial room temperature low-pass filter circuit, and then two stages of cryogenic low-pass filters mentioned in section 4.1 before they are passed to the chip contact pads by adjustable wafer probes.

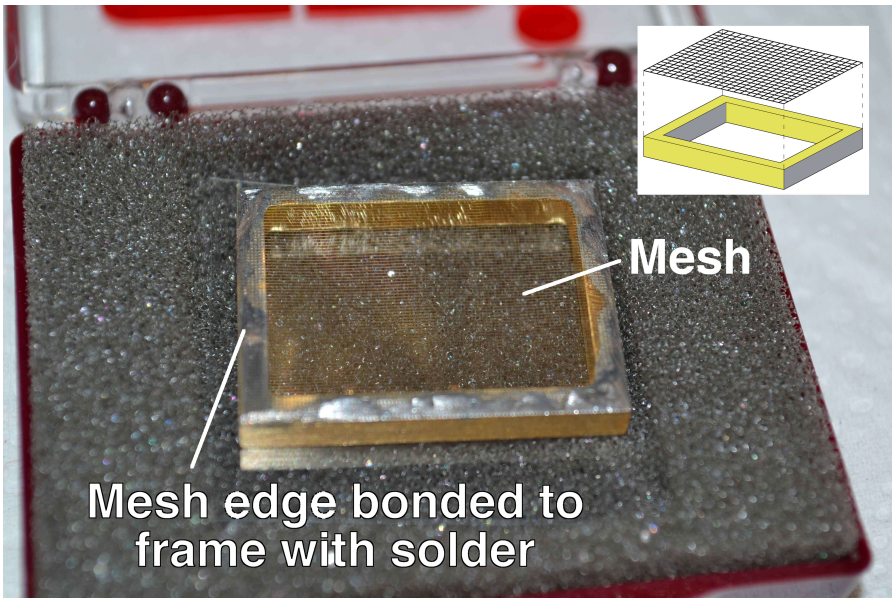
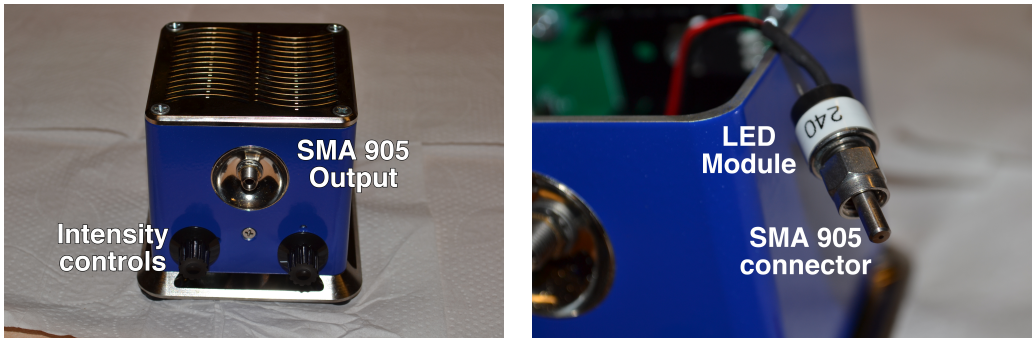


FIGURE 4.10: The mesh window that comprises one wall of the MW screening chamber. The window is designed to fit into a corresponding slot in the bottom of the cryogenic chamber, and is held in electrical contact with the inner walls of chamber bulk. The window mesh and frame are both made from copper, soldered together. The holes in the mesh are approximately 234µm square, separated by a copper grid with strand thickness 19.8µm, giving an open area of 85%.

4.6 The Ultra Violet Source

Rather than inject electrons using an established method, a space saving electron injection technique has been chosen which uses UV light at 240nm to strip electrons directly from the surface and walls of the set up. The light is generated at the room temperature flange by a 240nm LED source, producing 24.2µW (*Ocean Optics*). The fibre optics used to guide have a rated loss of 1.2dB, or approximately 24%, and it can be estimated that the number of photons n per second arriving at the end of the fibre is equal to $0.76 \times P\lambda/hc = 2.2 \times 10^{13}$.



(a) (b)

FIGURE 4.11: The UV light source is shown. The housing shown in figure 4.11(a) contains the LED, as well as the power supply and intensity controls. The LED itself is shown in figure 4.11(b).

To predict the energy of ejected photoelectrons it is necessary to equate the difference between incident photon energy, and the work function of the target metal. The crystal structure of gold can affect its work function [100], so for this calculation we will assume a target of pure polycrystalline gold, with a work function $\Phi_{\mathrm{Au}} = 5.1\mathrm{eV}$ [101]. As a condition of the photoelectric effect, a work function higher than the incident photon energy will yield no ejected electrons. A 240nm photon produced by the UV LED has an energy of $hf = 5.17\mathrm{eV}$. Compared to the accepted work function of gold Φ_{Au}, this yields an ejected electron energy of

$$hf - \Phi = 5.17\mathrm{eV} - 5.1\mathrm{eV} = 0.07\mathrm{eV} \tag{4.1}$$

Corresponding to an electron temperature of

$$T = 0.07e/k_{\mathrm{b}} = 812\mathrm{K} \tag{4.2}$$

In the 'Geonium Chip' however the surface is a mix of Au and Ag at ratio of 80% Gold to 20% Silver, with the exception of four test chips made with pure gold metallisation. This mix has an effect on the work function of the surface, and it becomes a function of the two metals observed in [102] to approximately follow the relation $\Phi = \Phi_{\mathrm{Au}} + 0.91(p^2 - 1)$ where p is the fractional percentage of gold (in this case 0.8), thus the work function reduces to around 4.8, giving an initial electron energy of 0.4eV and a temperature of $\simeq$ 4600K from the same frequency photon.

The light is guided to the trap with 600µm step-index fibre, and aimed such that the majority of the trap electrodes and chamber walls are within the numerical aperture of the fibre. It was decided not to use any lens after the fibre to focus the light to reduce the level of complication in the set up. Held by an open ended SMA905 adapter, the fibre is positioned such that it illuminates the side wall, back wall, and the surface of the chip inside the cryogenic chamber, ensuring a cloud of electrons will be generated when the UV is applied.

Compared to other electron injection systems, e.g. field emission points [103] or thermionic sources [104, 105], injecting electrons with the photoelectric effect offers certain advantages, the most notable is that it removes the need for additional electrodes, or emission points, which may require large voltage gradients to stimulate electron emission. After emission the electron passes through the gradient, and as a result is imparted with many hundred if not thousands of eV of energy which have to be dealt with accordingly. While this energy is not necessarily an issue in terms of capture, as systems using FEPs routinely demonstrate this ability, however if the system is to be scalable then high voltage sources are best avoided to simplify the electronics. The electrons injected by UV are limited by the energy of the photons, and as such will not exceed the 0.07eV energy stated in equation 4.1, so if higher energy electrons are required [106] then it is not possible with this method. For a thermionic source, a hot cathode must be present near the trapping volume in order to emit electrons, but again this method requires some internal wiring and structure in order to supply current to the cathode, and aperture to let the electrons in the trapping volume. The primary disadvantage of using UV light is the requirement of the optical access, which requires shielding from the trapping volume.

After leaving the fibre, the ultra-violet light passes through a quartz window, and a fine metallic mesh to reach the trap seen in figure 4.10. With the electrostatic potential off, the UV liberates a diffuse cloud of electrons which follow the curvature of the magnetic field lines, until the confining potentials are activated. Any electrons not in the trapping volume are lost. Results from SIMION simulations can be seen in section 2.5.1.

Chapter 5

In-House Manufacture Techniques

The desire to keep as much of the manufacturing process entirely within the laboratory as possible was motivated initially by the cost and lead-times associated with having the work performed by external workshops. For example, one quote for a chamber build was over double the cost of buying a CNC table for ourselves. However there were downsides, we were limited by budget to an entry level machine, and our group contains no trained machinists. Thus, the overall quality of finish and machining tolerances were less than what could be expected from a professional machine shop. It was also necessary to learn many things. From the basics of how to use the machine and set the correct co-ordinate system, to what the correct feeds and speeds for each tool diameter, tool material, tool type, number of teeth, stock material etc. Many of these things are best learned through workshop experience and cannot easily be learned from written texts. Thankfully, there are many online resources with extensive forums and discussions, designed for hobbiests and small project users, as well as inexpensive software and calculators to help bridge the knowledge gap.

5.1 CNC Router

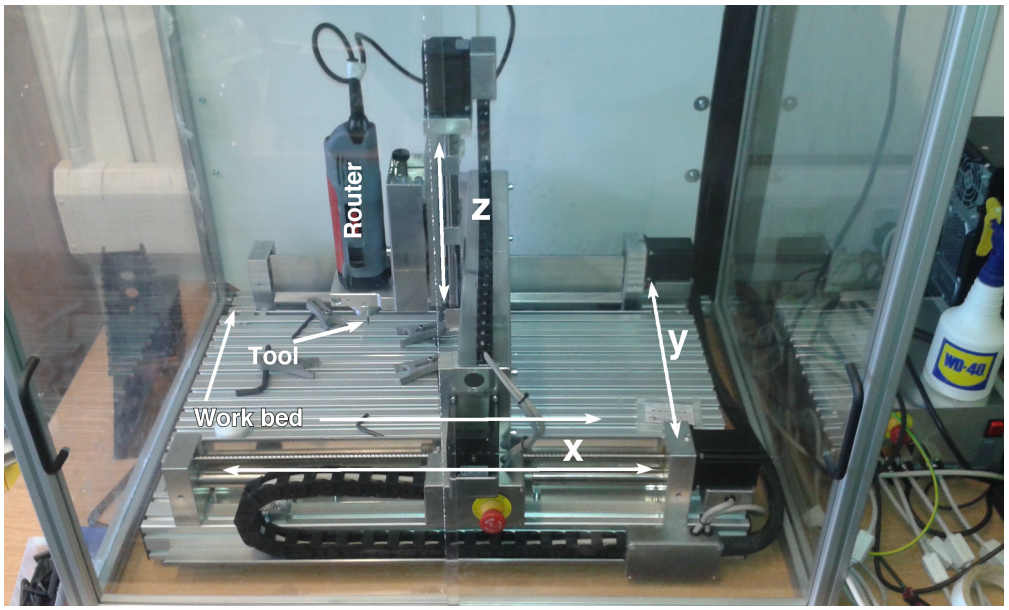


FIGURE 5.1: A picture of the High-Z CNC table, and the enclosing perspex housing necessary to contain any flying chips etc.

The machine purchased was a *High-Z* CNC table, with full 3-axis movement, later upgraded with a removable turntable to allow for 4-axis builds (this proved particularly useful for cutting spools for magnetic coil winding). The stepper motors and gearing give a 1.87µm movement resolution over the working x, y, z area of 400mm × 300mm × 110mm, however other components (bearings, guideways etc.) limit the repeatability to to approximately 20µm The table was mounted with a *Kress* 1050W router, capable of rotational speeds from 5,000 to 25,000 rpm and holding a tool shank diameter of up to 8mm. The collet could hold any round-shanked tool, and thus with the appropriate tooling the router can work with most conventional materials, including ferrous and non-ferrous metals, glass fibres (e.g. circuit boards) and composites.

One machine limitation we found was when using micro end-mills of below $\simeq$ 100µm diameter (tools down to 20µm were tested), as the run out and vibrations of the machine were comparable to the tool diameter, and resulted in damage to the tool after only a short while. To make use of these extra small tools it would be necessary to purchase a more specialist machine.

5.1.1 Machining Considerations

The mechanical action of material removal generates a large amount of excess heat, which can be problematic if left unchecked, causing damage to the tool and work piece. It is not difficult to exceed the melting temperature of soft metals such as aluminium if heat is allowed to build, and metals such as oxygen-free copper have a tendency to grab the tool, leading to breakage, particularly with smaller tool bits. Heating can be controlled in a number of ways:

- **Tool Engagement** Adjusting feeds, speeds, and depth of cut should be the first priority when controlling heat. Too fast and too much 'chip load' on a tool will result in a rapid build up of heat, as well as a poor finish. Too slow and the tool can be susceptible to 'rubbing', where the chip load is too low and the friction of multiple cuts to the same surface volume causes a build up of heat. This then means that the correct rates lie between those two, and should be calculated before cutting. The feeds and speeds also vary with the number of teeth (or 'flutes') a tool has. For example: in one instance a 4 flute tool was being used in aluminium with the feeds and speeds better suited to a 2 flute tool. This meant that the tool was engaging the material twice as often as previously, and the resulting friction caused the aluminium stock to melt, welding to the tool - which then had to be discarded.

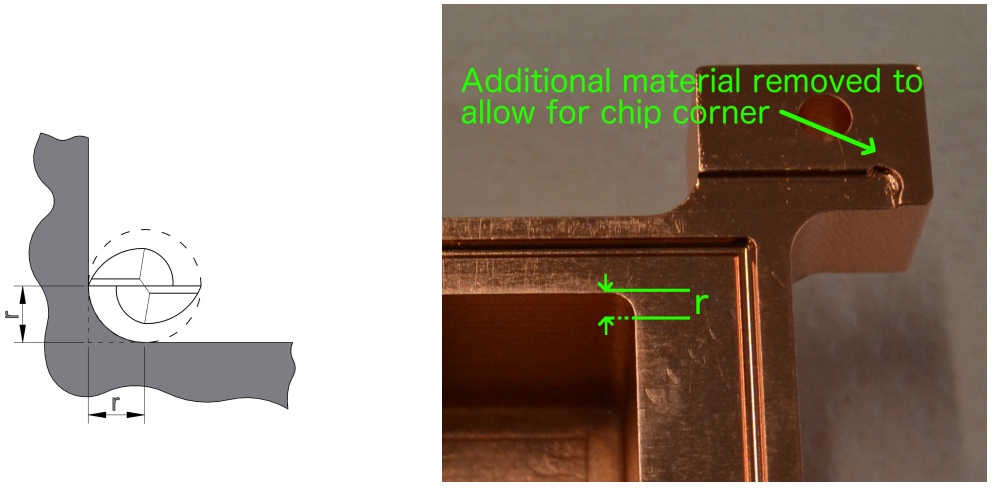
- **Chip Clearance** Following on from tool engagement, once cut, the metal chips must be removed as quickly as possible. Heat is stored within the chip, and so chip ejection has the effect of removing heat and cooling the cut. If chips are allowed to pile, the system stays hot and chips are at the risk of being re-cut over and over, which can cause them to melt and damage the tool and work piece. Tools with lower numbers of teeth are better able to eject chips as they have a more open area along the helix for chips to travel. Steeper helix angles on the cutters also give better ejection rates. For this reason cutters with 2 or 1 flutes and high helix angles were favoured when cutting aluminium.

- **Lubrication and Coolant** Perhaps the simplest method is to apply lubricant to the cutter and work piece. Not only does the lubricant reduce the friction during the

cut - which has the added benefit of prolonging tool lifetime - but it also provides a liquid coolant to extract heat from the area. The most popular method is known as 'flood coolant' where a thin, low viscosity lubricant is applied constantly throughout the cutting, keeping temperatures low. Unfortunately, flood coolant was impractical for our machine, as well as expensive to set up. Instead we opted for manual application of a light oil, in this case the commonly available *WD-40* bought in 5 litre bulk containers to keep costs down. In a specialist instance (cutting OFHC copper with a 2mm end mill) the work piece temperature was kept down by pouring chipped dry-ice over the stock during machining. The low temperature of the dry-ice meant that the copper stayed brittle, and resisted tool grabbing.

- **Roughing Bits** A roughing bit or 'chip breaker' is a tool with a patterned cutting edge, designed to cut a number of smaller chips per tooth rather than one larger one. The finish given by these bits is poor, and they are best suited to removing bulk volumes of material and non-critical faces, and require a tool change for a finishing pass if a higher quality finish is desired. In many applications these are simply used to speed up production by allowing faster material removal, however they are also useful in applications where it is necessary to control temperature levels.

Milling or routing has its disadvantages. One such disadvantage is that it is best suited for milling designs with external angled geometry, and any internal angles are subject to a minimum radius of machining (a sketch is shown in figure 5.2). If the application requires use of the corners, for example if a square cornered object must fit into the cut like in the Geonium Chip alignment recess shown in 5.2(b), additional material can be removed to make room for the squared corners.



(a) (b)

FIGURE 5.2: 5.2(a) is explanatory sketch of what is meant by a 'minimum corner radius', as dictated by the tool diameter. 5.2(b) is an example of the tooling limitations experienced while manufacturing the Geonium Chip vacuum chamber. In order to fit the square-cornered Geonium Chip into the recess, additional material had to be removed in the corners.

5.1.2 Control Software

To interface with the machine, appropriate software is required to read the 'G-code' - a set of commands and co-ordinates, read by the software and outputted to the controller. A sketch of the setup can be seen in 5.3. The software runs on a regular 32-bit windows system, and is able to accept G-code in all common formats, including simple text files. It also doubles as a code editor if the code needs to be altered on-the-fly, and has the ability to input individual commands one-by-one as required. Other useful features include a run-time estimate function, and a number of G-code generators to quickly create code for simple geometries such as rectangular or round pockets etc.

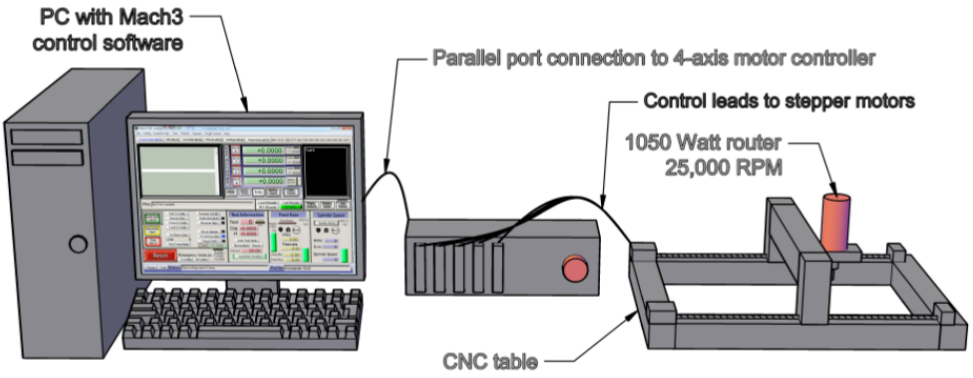


FIGURE 5.3: Shown is a sketch of the CNC setup. It is a simple arrangement of a normal Windows PC, stepper motor controller box and x, y, z table, with the router mounted as standard.

5.2 Cryogenic Chamber

The cryogenic chamber discussed in section 4.4 was manufactured in house by the CNC described in 5.1, and was milled from a single piece of aluminium. This section contains a discussion of the design process as well as some information about sealing the chip to the chamber with indium.

5.2.1 Design Process

Presented in this next section are a few of the designs considered and eventually modified or discounted as part of the design process.

The first designs echoed previous successful Penning trap systems which utilise a cylindrical cryogenic vacuum canister to encompass the experimental region. The advantage of this lay mainly with the comparatively low level of complexity involved in the construction of the cannister, consisting of a simple vacuum can and indium flange. A cannister like this however required a number of cryo-compatible electronic feedthroughs, as well as at least one feedthrough for the UV light used for electron preparation (see section 4.6). If a window was to be put on the cannister flange then the issue of space taken up by the window would mean difficulty fitting other wiring feedthroughs into the same space.

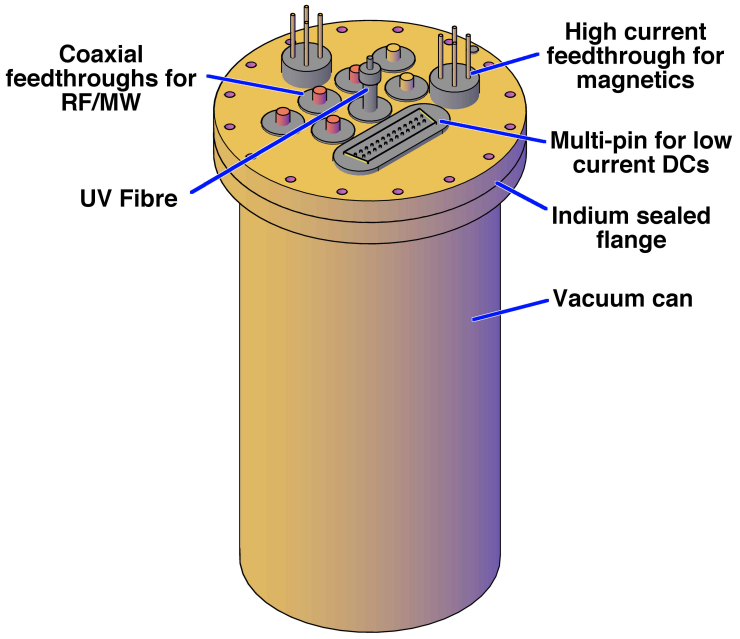


FIGURE 5.4: A sketch of the can-style vacuum chamber inspired by previous successful Penning trap experiments. All vacuum chambers were designed to be semi permanently sealed with indium and, and evacuated through a pinch-off tube. In this design, the feedthrough flange is crowded, making it difficult to access wiring. Later versions of the chip had simplified feedthrough requirements.

The next major design step was a switch to a more compact, form fitting design, with the resonant MW screening chamber incorporated into the vacuum structure. This feature was maintained in various manifestations until the final chamber version, and the first examples can be seen in figure 5.5. Up until this point, the MW screening chamber had been a separate piece, contained within a larger vacuum structure. Throughout this process, the Geonium Chip design had not been finalised, so such features as a 'chip holder' can be seen in figure 5.5(c). The idea of this was to allow easy switching of chip designs from a more permanent holder. The Holder would take some strain away from the chip substrate, and form part of the vacuum chamber. The idea was abandoned in later designs due to concerns about alignment and surface continuity involved with having the chip on a separate substrate. Other defunct features include the magnetic coil array, shown throughout figure 5.5 as a magenta place-holder. At the time of designing the chamber, the theory of the coil array (section 2.4) had been largely worked out, but the end size and design of the coils had not been finalised. Thus a rectangular block was used, large enough to be a catch-all, and then modified as the coil design progressed, for example in figure 5.5(e) where a more advanced coil structure is shown.

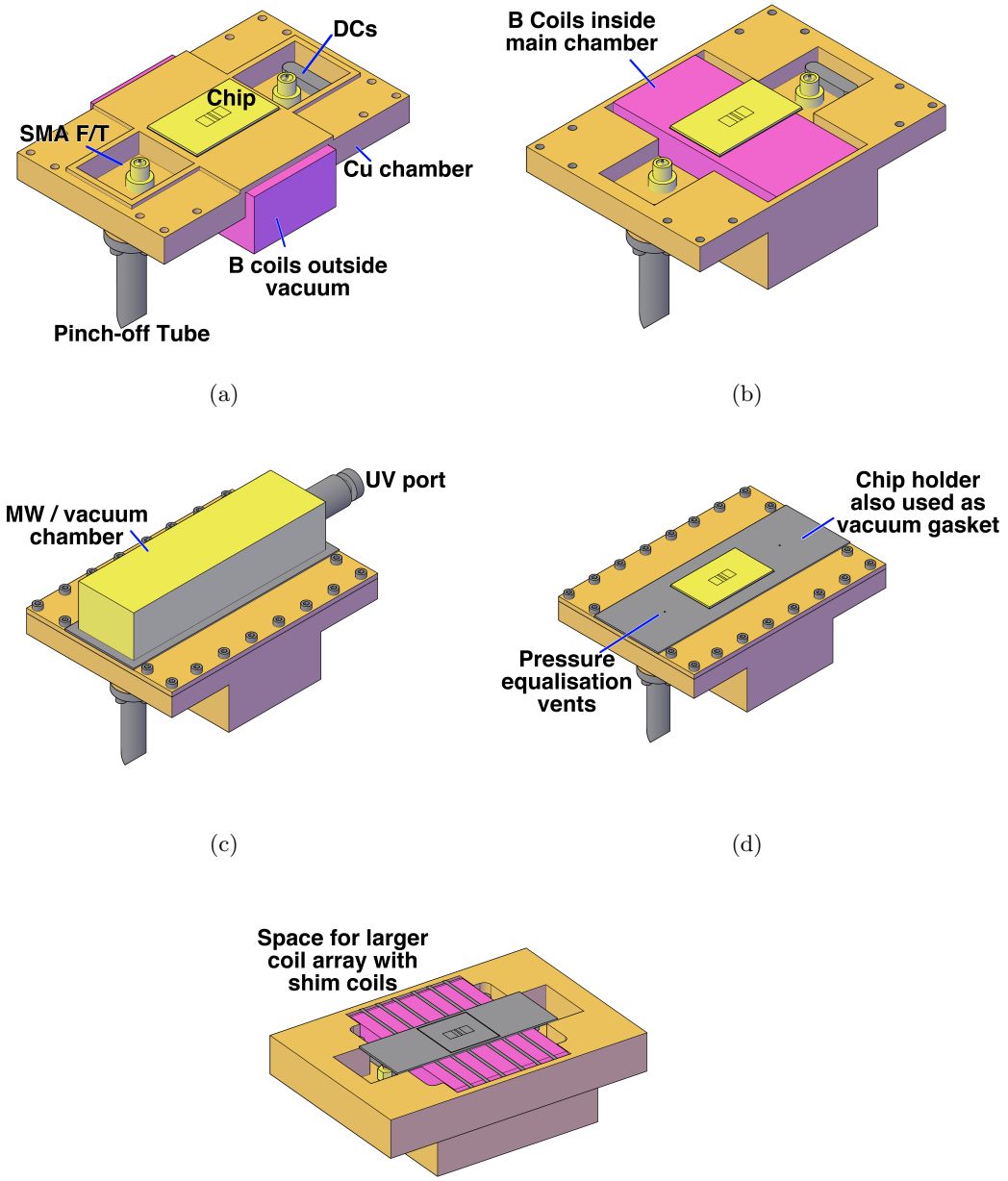
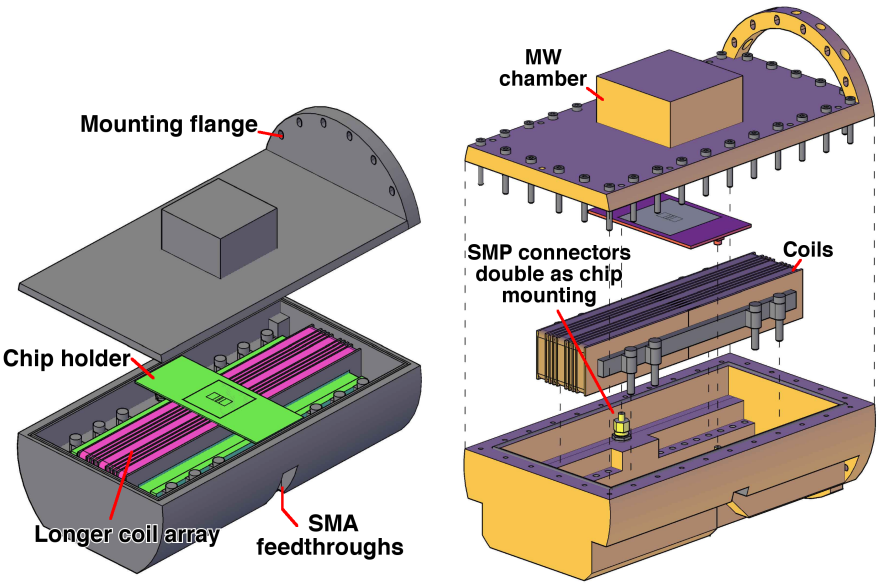
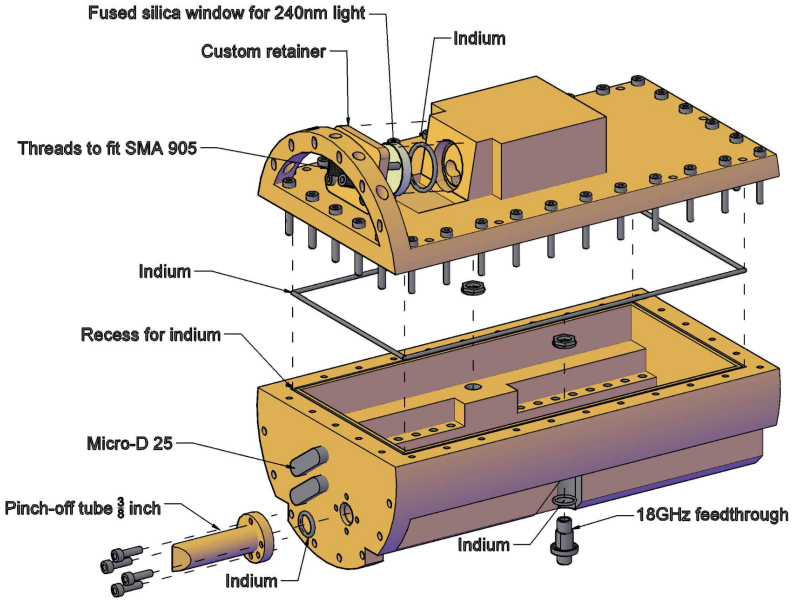


FIGURE 5.5: Cut-away views of a closer-fit vacuum vessel. Version 5.5(a) shows the chamber with the magnetic coil array - represented by a the magenta place-holder - mounted outside of the cryo-vacuum region. All variations share a few key principles, including a MW screening box shown in 5.5(c), and a 'chip holder' shown grey in 5.5(d). The purpose of this was to provide strain relief, support, and a method of electrical connection to the chip electrodes. It was intended that it would be a permanent fixture, and the chip electrodes would be swapped in and out as desired. RF and DC were fed through from the bottom, requiring some internal wiring to connect the chip. A progression step of the magnetic coil array is shown in 5.5(e), where the place-holder has been given some basic coil shape and mountings.

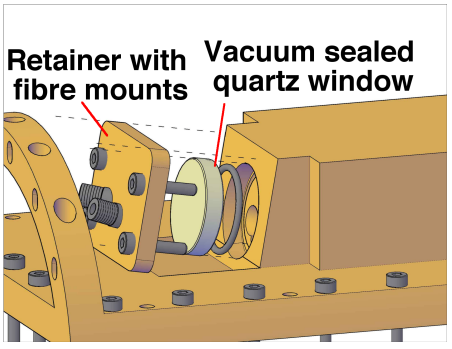
In 5.6 the design was elongated and rotated 90° to allow for longer magnetic coils to lie vertically in the main experimental volume. The overall concept was similar to 5.5, sharing a number of similarities, including a vacuum vessel with integrated MW screening chamber, chip-holder based mountings, and magnetic coils within the vacuum region, and required vacuum feedthroughs for the electrical connections. A mounting flange was incorporated into the design, to remove the necessity of any further mounting structure. Designed to be cut from a single 120mm diameter piece of OFHC copper. The downside of this was not only the initial cost of such a large piece of copper, but the difficulty of machining OFHC copper meant that the manufacturing was prohibitively expensive for such a complex piece. This turned out to be one of the main reasons for eventually choosing to manufacture the chamber in-house, as the cost of this chamber was far greater than buying the CNC router described in 5.1. Another downside to this design would be the sheer weight of the piece, as the necessary wall thickness to prevent buckling during evacuation would require a considerable weight (around 9kg) to be hung from the coldhead. This would put considerable strain on the structural components.



(a) (b)



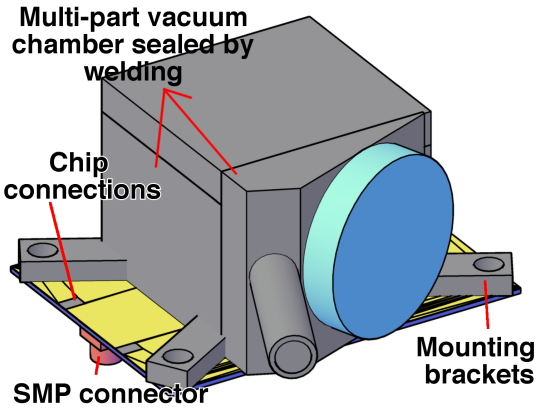
(c)



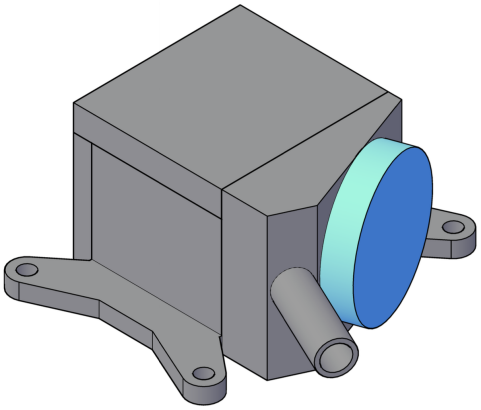
(d)

FIGURE 5.6: 5.6(a) and 5.6(b) show some views of the longer vacuum chamber which included a chamber mounting flange. The chamber design was refined in 5.6(c) and 5.6(d) to include UV insertion points, designed to hold the SMA fibre in a fixed position close to the inlet window.

The prohibitive cost of this chamber meant that a radical re-design was called for, drastically simplifying the chamber. Inspired by on-chip vacuum chambers [95], the decision was made to do-away with vacuum feedthroughs altogether, and instead have part of the chip extend beyond the evacuated region. This supplied a means of connection to the chip electrodes via the buried wires included in the chip as part of the microfabrication. The chip would be indium sealed to the chamber, and hold the vacuum with the substrate of the chip. This choice carried a number of risks, as there are very few comparable systems. The 675µm silicon wafer substrate is very fragile, and not designed to withstand a great deal of mechanical stress. This limited the size of the MW screening chamber, as a large unsupported region would be prone to cracking under the atmospheric pressure [97] so a 20mm cube was chosen as it complied with the screening requirements, as well having a small enough face to support the silicon. Indium is soft when compared with other metals, but requires a certain amount of compressive force to deform. A poorly supported silicon chip will crack very easily so compressing the indium to form the seal must be done with great care. All these factors had to be considered when designing the chamber. As seen in figure 5.7, the first chamber designs were a multi-part design, designed to be welded together to achieve the final piece. The advantage of this would be that the MW screening box would have sharp corners on the inside surface. A machining limitation of milling bits is that it is not possible to mill a perfect right angle in the plane of rotation of the tool, as there is always material left as a fillet with the radius of the tool (corresponding to the four corners aligned with the y plane of the trap). As it was decided that the Q-factor of the MW screening cavity was less critical at this time, a fillet of 1.5mm radius was accepted, as this was the smallest radius tool we could acquire with the necessary length to cut the full chamber pocket.



(a)



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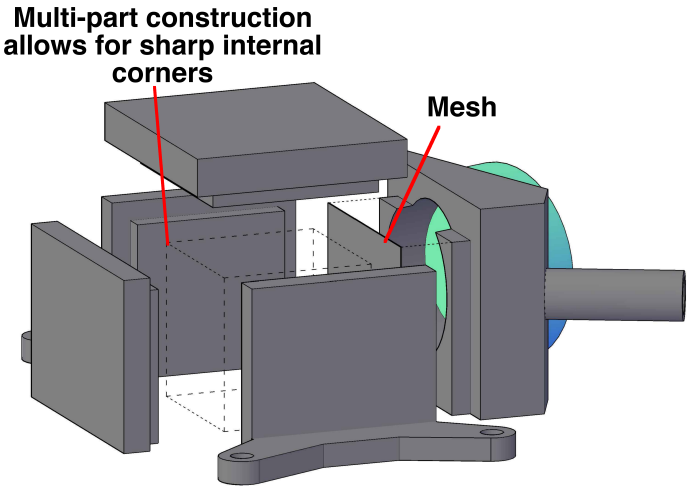


(c)

FIGURE 5.7: First formulations of the design which would become the final design for the Geonium chip. The main difference noticeable between these early versions is the size and shape of the mountings, which became thicker and wider as it became apparent that aluminium would be used, and so to prevent bending during indium compression, the mounts were bolstered. The Chamber was also first designed to be assembled from a number of pieces welded together, but this idea was discarded in favour of milling from a single piece.

5.2.2 Material Considerations

The choice of material to manufacture the cryogenic chamber was influenced by a number of factors. The goal was to have a system capable of rapid prototyping at low cost, without sacrificing the functionality of the devices created. Stainless steel performs very well as a vacuum vessel, but lacks the desired low conductivity electrical properties, as well as having a larger relative magnetic permeability when compared to non-ferrous metals [107]. Even the austentitic 3xx series of stainless steels have a small but significant μ_r, and when subjected to the physical stresses of machining, the crystal structure can alter to the arrangement of ferrite or martensite, both of which are highly magnetic [107, 108].

A common material choice for applications similar to this experiment is copper, specifically oxygen-free high conductivity copper (OFHC), which is a high purity electrolytically refined metal [109], popular for its electronic and thermal conductive properties. In many ways this material would have been an ideal candidate, were it not for the difficulty of machining, which renders it unsuitable for rapid prototype-style manufacture. The cost of material is also a factor, being an order of magnitude higher than aluminium alloys, and if specification certification is desired then this can increase the price further.

The material chosen for the manufacture of the chamber was 6061 aluminium. The reasons for choosing this have largely been detailed in previous paragraphs, but it was largely governed by our desire for rapid, easy manufacture, with a low price-tag. Aluminium fulfilled all these criteria, with good electrical and thermal conductivity, however it has a number of downsides. The first and foremost is aluminium's affinity for oxygen. It is highly reactive, and readily forms an oxide barrier layer almost immediately after exposure to air. Aluminium oxide itself is fairly chemically stable, and a useful substance in many areas as component of sapphire and alumina, it has found uses as a high frequency substrate or as an industrial abrasive close to diamond in hardness. However the presence of dielectric is unacceptable in the Geonium Chip housing as it would collect static charge, and distort the electric potential. Oxidation is also of concern for copper, but the reaction takes place much more slowly and is much less of a problem to remove during surface preparations. For both materials then, it is necessary to plate the surface with an inert barrier of pure gold. The barrier layer of oxide makes this process

non-trivial with aluminium, requiring a number of preparation steps detailed in section 5.3.1.

5.2.3 Indium Gasket Test

It was necessary to test the indium sealing technique, as it was not known how the chip would react to undergoing the compression necessary to form a hermetic indium seal. Most literature on the subject of indium sealing deals with thick metal flanges which hold the tensions and pressures required to deform the indium, and spread it evenly. Due to the brittle nature of silicon, it is essential that it experiences no bending or uneven pressure, or the wafer will simply snap. The solution chosen was to fully support the wafer with a plate of metal approximately 15mm in thickness, and apply the tension to it instead. This spreads the pressure throughout the whole face of the silicon without bending. To ensure good alignment, the compression plate had a shallow recess with the same dimensions as the Geonium Chip.

The indium came as a 1.6mm diameter wire, which was degreased with ethanol and formed into the 0.8mm deep recess cut into the chamber. To join the two ends of the wire and finish the loop, the wire was simply twisted, and gently pre-compressed to make it the same height as the rest of the wire, and then the excess wire at either end is removed. Ideally an indium flange would have an alignment lip, allowing it to be pressed between two flat sealing surfaces, but this was not possible when using a silicon chip for one face, as the profile of the surface is fixed, and no recess could be cut into the silicon. Thus a recessed groove was cut in the aluminium face, which meant the sealing process required a little bit more care to prepare. When compressed, fresh indium is exposed from the wire bulk, and the clean, oxide-free metal wets and bonds to the surfaces of the chip and the chamber, forming a hermetic seal. Indium readily wets most materials, hence its popularity as a solder for difficult materials.

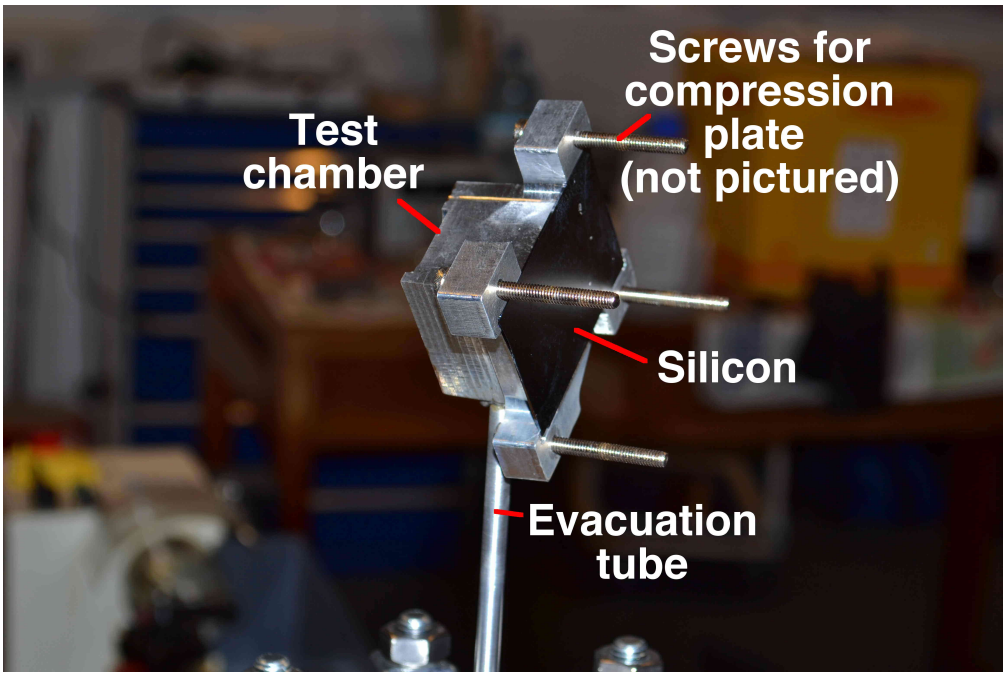


FIGURE 5.8: Shown is a test of the indium seal between a prototype chamber and a silicon wafer. The clamp used to compress the indium has been removed, and the silicon is being held by the indium, and by the atmospheric pressure. Even after breaking the vacuum, the silicon is still held extremely firmly, and was difficult to remove without breaking the wafer. The best technique was found to be gently heating the seal to soften the indium. The basic version of the chamber shown had no window, and the pinch-off tube is held by vacuum epoxy sealant. The system achieved a vacuum level of around 5×10^{-8}mbar

5.3 In-House Electroplating

The electroplating of components was also performed in-house, and thus it was possible to have pieces machined, cleaned and gold plated quickly and cheaply. Electroplating can be difficult to perfect, with a lot of trial and error was involved in find the best chemicals, cleaning steps, and current densities required to obtain a good finish. With that in mind, the results achieved were done so with some fairly rudimentary equipment (see 5.11). Once a method was established, it is simply a matter of following the steps and a good finish can be achieved every time, completing the rapid manufacture process.

The primary objective of the procedures covered in this section are to achieve a good quality gold plate on any pieces manufactured in-house, without the need to send off to an external plating shop. Thus, the majority of the following points relate directly to plating gold on aluminium, though the plating equipment can be used on a range of metals, including copper PCB cladding, and superconductors to facilitate conventional

soldering techniques on otherwise difficult to solder metals. Of the plated metals in this section, aluminium is by far the most involved and technical, requiring the most pre-plating steps. Copper and silver can simply be plated after a simple corrosion and grease removal, and so are not covered in detail.

Gold has excellent electrical properties, but particularly useful is its extreme nobility, that is to say it is very unreactive, and thus will maintain its electrical properties regardless of exposure to air etc. The corrosion resistance of gold plays an important part in cryogenic systems, as mentioned in chapter 4. Heat flow between conductors is hindered by oxidation or other corrosions, thus a gold plate will ensure that the thermal transport across the interface is not hindered.

5.3.1 Surface Preparation

By far the most important step of the plating process is the preparation of the metal surface prior to immersion in the plating solution. Due to the chemistry of different metals, each metal reacts with each plating solution differently, and requires research prior to embarking on the plate process. One common feature of all processes is that any piece to be plated must be free of dirt, oils, greases, oxides, glues, soap residues, etc., or the process will yield poor results, or not work at all. This is not a trivial task, parts may include difficult to clean regions, for example small threaded holes or fragile meshes. Even seemingly small things such as handling an un-cleaned component before handling a cleaned component can transfer dirt from one to the other and contaminate the gloves, requiring a change. Any cleaning steps are best performed with minimal time in-between to reduce the risk of contamination between stages.

- **Oxides and Surface Corrosion** If the piece has been out in air for a prolonged period of time, as is common for metal stock from a supplier, the piece will likely need first require a mechanical oxide removal. This can be done by any suitable method, *Scotchbrite* pads were found to work particularly well as they had good abrasion but were not so aggressive that they left deep scratches or removed small features. Conventional sandpaper is also effective. Figure 5.9 includes an example of the finish after this step.

- **Polishing** For an optimal finish, the metal can be polished after corrosion removal, for a mirror shine. While not strictly necessary for most applications, it can be useful for applications such as high-Q resonators, and pieces which require good thermal contact between surfaces. The overall finish of any subsequent plating is also more visually appealing. An example can be seen in 5.9

- **Desmutting and Degreasing** An ultra-sonic cleaning bath to remove the bulk of the dirt and grease. Pieces were submerged in hot $(40 - 50°\text{C})$ clean water with a moderate soap solution, stirring periodically. This stage was repeated until visually clean, and then rinsed in clean water to remove any soap. A chemical degreasing in acetone followed, then followed by a de-ionized water rinse to remove any residuals still left on the piece.

- **Other Specialised Surface Preparation** Due to its affinity for oxygen, plating onto aluminium requires a few specialised surface preparation steps, which will be detailed in section 5.3.2. A mix of phosphoric acid, acetic acid and a surfactant (*AL65 solution - PMD Chemicals*) was used as a chemical oxide, grease and general dirt removal step, for where it was not feasible to mechanically remove the surface corrosion. Next the piece is immersed in a zinc-hydroxide solution, for a process known as 'zincating' (details in section 5.3.2). A chemical process where the zinc supplants the surface aluminium, and is deposited on the surface of the aluminium. For best results it was found that a 'double zincate' yielded the best results, wherein the first layer of zinc is partially removed with a weak nitric acid solution, and then the piece is immersed in the zincate solution again. This is done as zinc oxidises less readily than aluminium, and provides a barrier layer onto which the rest of the plating process is simpler.

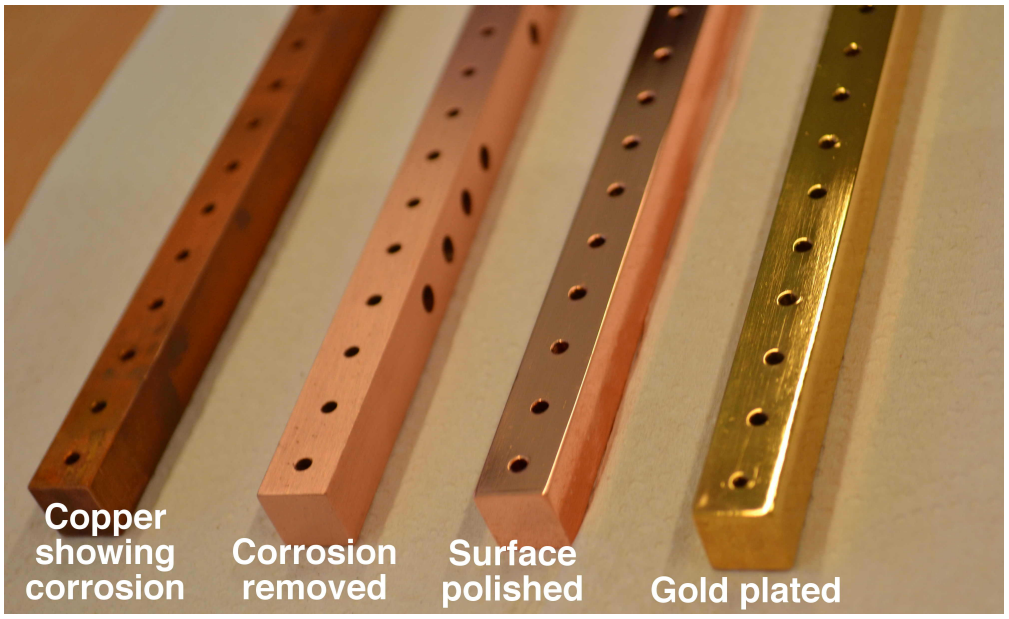


FIGURE 5.9: A comparison of surface preparations. From left to right: 1) Corroded copper strut, as a result of being left unplated in air for an extended period of time. The oxide layer is clearly visible. 2) Copper strut after abrasive treatment, the pinkish colour of fresh copper can be seen. 3) Copper polished to a mirror finish on a stitched-cotton wheel, and cleaned of dirt and grease. 4) Gold plate on polished copper.

5.3.2 Zincating

The process of zincating aluminium is common practice in industry as a plating preparation. The zincating is an electroless plate process [110], i.e. no current sources are required as it is a displacement reaction with the following equation

$$3\mathrm{Zn(OH)}_4^{-2} + 2\mathrm{Al} \rightarrow 3\mathrm{Zn} + 2\mathrm{Al(OH)}_4^{-} + 4\mathrm{OH}^{-} \tag{5.1}$$

The reaction takes place quickly, with only 30 seconds or so required. If the reaction is left longer, the zinc layer becomes thick and spongy in texture, giving a poor finish, and regions prone to blistering of subsequent plating steps. A solution to this is to perform a 'double zincate', where the first layer of zinc is partially stripped with a weak nitric acid solution, and then zincated a second time. This leads to smaller, overlapping crystals forming in the zinc layer, yielding a smoother, more desirable finish [111].

Nitric acid strip (also known as de-smut solution) was mixed to the correct concentration C from standard 70% concentration nitric acid. The desired concentration was $C = 50\%$

by weight per unit volume V, and so the following dilution was performed

$$C_1V_1 = C_2V_2$$

where:

$$C = \frac{(\text{percentage by weight}) \cdot (\text{density}(\text{g} \cdot \text{ml}^{-1}))}{\text{formula weight}(\text{g/mol})} \times 10$$

$$C_{70} = \frac{70 \cdot 1.413}{63.01} \times 10 = 15.7$$
$$C_{50} = \frac{50 \cdot 1.413}{63.01} \times 10 = 11.21$$

thus for 250ml de-smut solution:

$$V_{50} = \frac{11.21 \cdot 0.25}{15.7} = 0.1785\text{l} = 179\text{ml}$$

Once topped up with the remaining 71ml de-ionized water to 250ml, the de-smut solution was at the required strength, and the piece immersed for 1 minute, before the final zincation step.

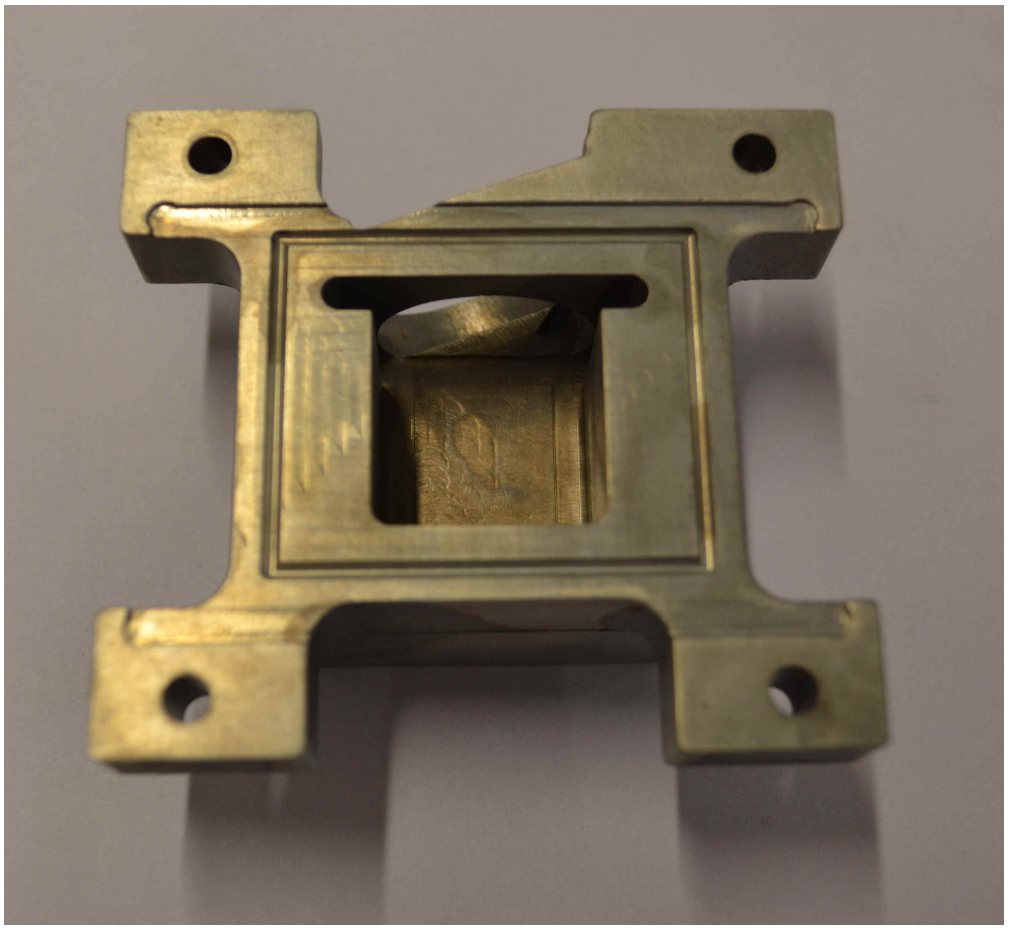


FIGURE 5.10: A view of the cryogenic chamber after zincation. It is visually similar to the bare aluminium before, however the metal is a darker grey colour from the zinc layer.

To prevent a patchy, uneven zincate, the piece must be rinsed as soon as it is removed from the zincate solution, as the solution will pool and continue to act on the piece in those regions.

5.3.3 Copper Plating

In the lab were two methods of electroplating copper. It was used as pre-plate to provide a barrier layer between the zinc and gold plate. Zinc and gold readily inter-diffuse, and are not recommended for direct plating. Copper was chosen rather than ferromagnetic nickel, as the plating would be surrounding the electron trapping region, and thus any magnetic materials in this region were to be avoided. Without this barrier layer of nickel, eventually the copper will diffuse into the final gold-plate, and need to be re-finished. However, this is likely to take a number of years at room temperature [112].

- **Acid Copper** Initially, a common copper-sulphate based acid copper bath was used, as it is cheaply and easily available, and the acidity of the solution serves to remove some oxidation during the plate process itself, leading to good adhesion on most commonly plated metals. The bath itself comprises of 0.9kg dissolved in 4 litres of de-ionized water, and topped up with 38% sulphuric acid and 'brighteners' (chemical additives designed to break the crystal structure up, making a shiny finish) giving 5 litres in total.

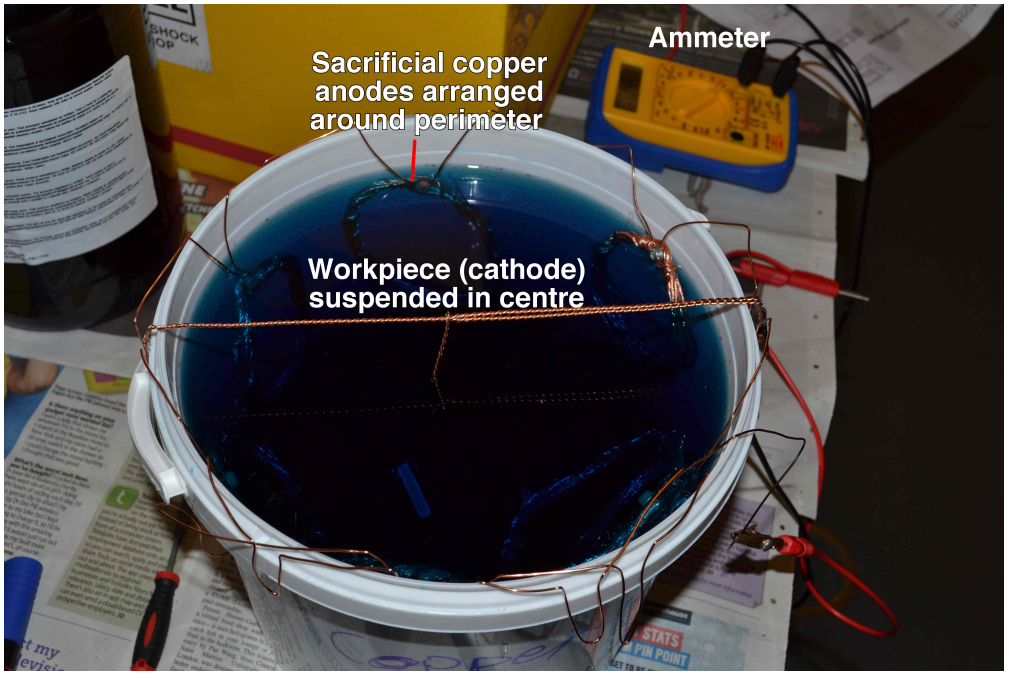


FIGURE 5.11: The copper sulphate bath used for acid-copper plating. Consisting of a five litre plastic bucket and a circular anode to give even coverage, made from re-purposed electrical wiring. Though it may appear rudimentary, the set up yielded consistently good results. The current was supplied by a bench-top power supply and monitored with a handheld multimeter.

This set up gave good results when plating metals such as nickel, silver, and NbTi (the latter two were used to enable ease of soldering to otherwise difficult metals).

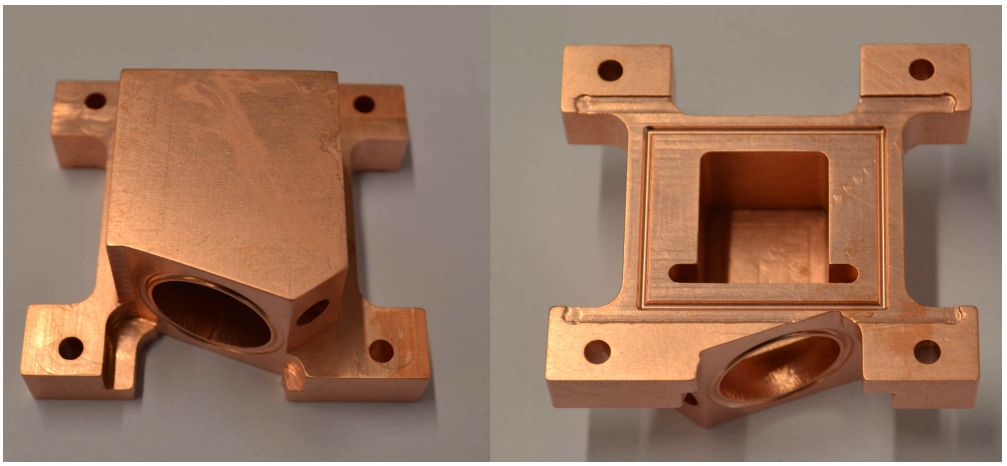
However, problems arose when attempting to plate zincated aluminium, as the interaction between the acid compounds and the aluminium caused blistering and peeling of the zinc layer, and attacked the metal itself, leaving 'pitting' (small regions of local erosion), shown in figure 5.12. This was determined to be caused by pockets of low current density [110], and can be seen in figure 5.12(a). The edges and external corners of the piece have the highest current density and have a good plate, whereas the internal corners, and flat faces of the piece have a blistered,

pitted appearance, and very little coverage. To remedy this, a plating formula specially designed for zincated parts should be used.

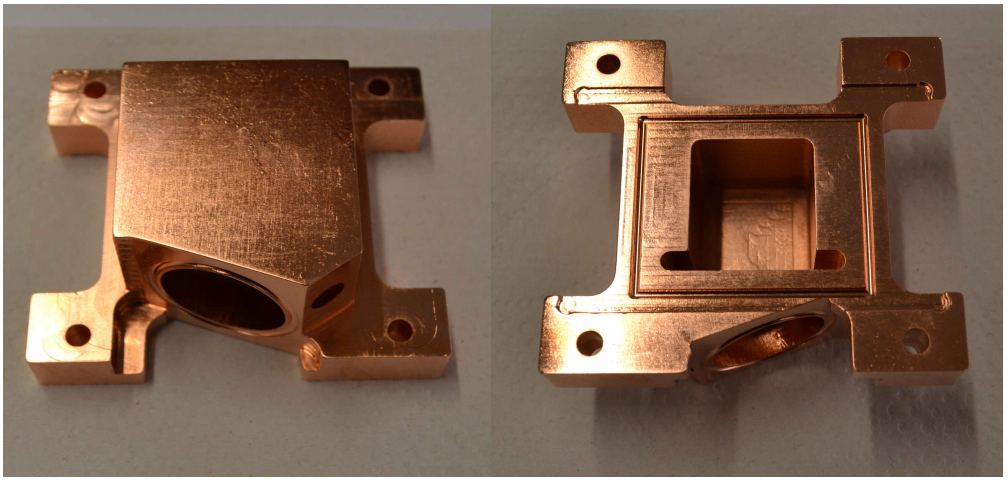
(a) (b)

FIGURE 5.12: Examples of failed attempts to plate acid copper onto zincated pieces. Figure 5.12(a) shows blistering and poor coverage left after the acid copper stage. Figure 5.12(b) shows the pitting left after the plate had been removed with abrasives.

- **Alkaline Copper** A specially formulated alkaline copper solution was acquired to remedy the problems associated with the acid copper bath. This was surprisingly hard to obtain, as the industry preference is for cyanide baths as these have better 'throwing power' (weight of copper deposited per unit current). Cyanide baths have acute health risks and specialist waste disposal requirements, making it unsuitable for our purposes. Non-cyanide alternatives are available, though proved hard to find in small enough quantities for non-industrial scale use. A pyrophosphate based bath was opted for and acquired from *Electrochemical Products Inc*, and a similar set up to that of figure 5.11 was employed, with the same circular anode design. The plating results were much cleaner with this formulation, though exhibited a matte appearance due to the larger crystal size (there were no 'brighteners' in this formulation). An example can be seen in figure 5.13. The matte appearance of the phosphate copper proved problematic as the texture was carried through to the gold plate, giving a dull, mustard coloured finish (see figure 5.15. We found the best solution to this problem was to give a second copper plate of acid copper on top of the phosphate copper, as the phosphate shielded the zincate from the acid sulphate bath, and no pitting or blistering problems were experienced. The smaller crystals of the acid copper plate gave a reflective shine to the piece, which was transferred to the final gold plate stage, seen in 5.14.



(a)



(b)

FIGURE 5.13: Figure 5.13(a) shows the finish from the copper pyrophosphate bath, it can be seen to be rose-coloured and matte in appearance. To prevent the matte appearance being transferred to the gold plate, the piece is subject to an additional plating step in the acid copper bath, where the brighteners yield a fine, reflective finish which is then transmitted to the gold plate.

5.3.4 Gold Plating

Once the pre-plating process is completed, the gold plating is fairly straightforward, as gold plates readily onto copper. Gold plate solution was purchased from *Gold Plating Services*, initially in a small batch of around one litre (one US quart) and then as plating progressed a further 3.8 litres (one US gallon) was purchased. Due to the price of gold, a sacrificial gold anode is too expensive to be used as is the case with the copper baths, so a platinum plated titanium anode is used, as it is not used up by the process. Best results were achieved with gold plate solution between room temperature and 50°C. An

example of the finished plate can be seen in figure 5.14. The chamber was left to plate at a current of 160mA for approximately 20 minutes, which for a piece area of 143cm^2 equates to an estimated gold thickness of 1.3µm [113].

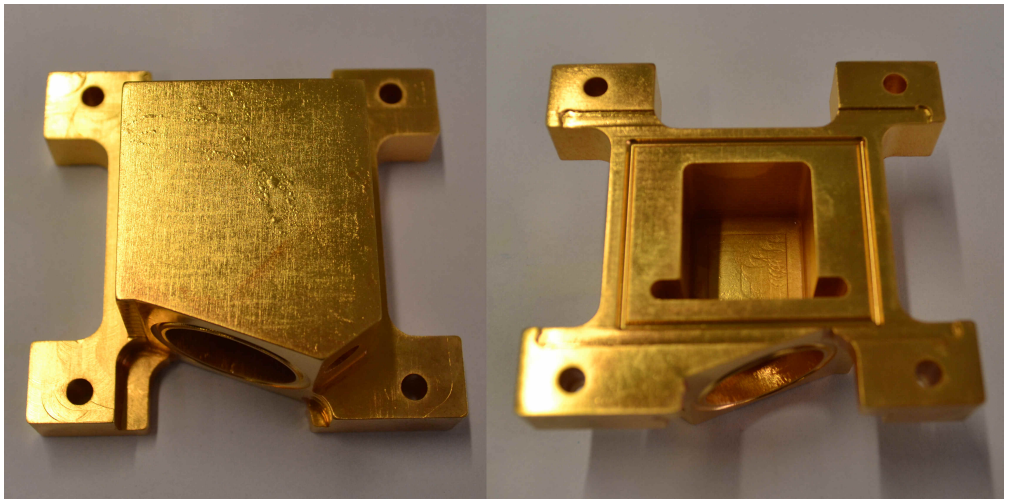


FIGURE 5.14: Gold plate finish on the aluminium chamber. This was the final step, completing the rapid prototyped chamber process.

FIGURE 5.15: Plating gold directly onto pyrophosphate copper yields good coverage, but a coarse, dull finish.

5.3.5 Plating Summary

Below is a summary of the steps undertaken to plate gold onto aluminium. It should be noted that the entire process should be performed with the appropriate safety precautions (lab coat, goggles, hand protection) which should be used at all times when dealing with potentially hazardous chemicals. If possible, completely avoid handling the piece, even with gloves. It is essential to rinse the piece in clean (or ideally de-ionized) water whenever transferring between two chemical baths, or cleaning stages, or the baths will become contaminated. There is a clean water rinse step between each of the following summary points.

1. Mechanically clean corrosion from the aluminium piece until fresh aluminium on show over the entire surface.
2. If a polished finish is desired, this is best performed at this stage, before the cleaning process.
3. Clean in an ultrasonic bath for as long as necessary to remove visible dirt, oils and polishing compounds.
4. Rinse with a solvent such as acetone or ethanol
5. Soak in deoxidiser/degreaser (*AL65, PMD Chemicals*) for 5 minutes.
6. Dip in the de-smut solution (see 5.3.2) for 30s.
7. Dip in zincate solution for 60s.
8. Repeat step 6.
9. Repeat step 7.
10. Electroplate in pyrophosphate copper for approximately 20 minutes at a suitable current*.
11. Electroplate in acid copper for approximately 20 minutes at a suitable current*, until the plate appears smooth and shiny.
12. Electroplate in gold solution for 5-20 minutes at a suitable current*, or until the desired thickness is achieved.

*The current to use depends on many factors, and may require some trial and error. The surface area of the piece, composition of the plate solution, and available metallic ions in the electrolyte all have an effect on the appropriate current. If in doubt, it is often better to plate for longer at lower current, to avoid stripping positive ions from the electrolyte solvents, which can tarnish the finish. For our chamber, it was found that 0.6A gave good results for the copper plate stages, and 0.16A for the gold plate stage. If the surface area of the piece is known, optimal anode currents can be found by using manufacture recommendation [113]

5.4 Other Machining

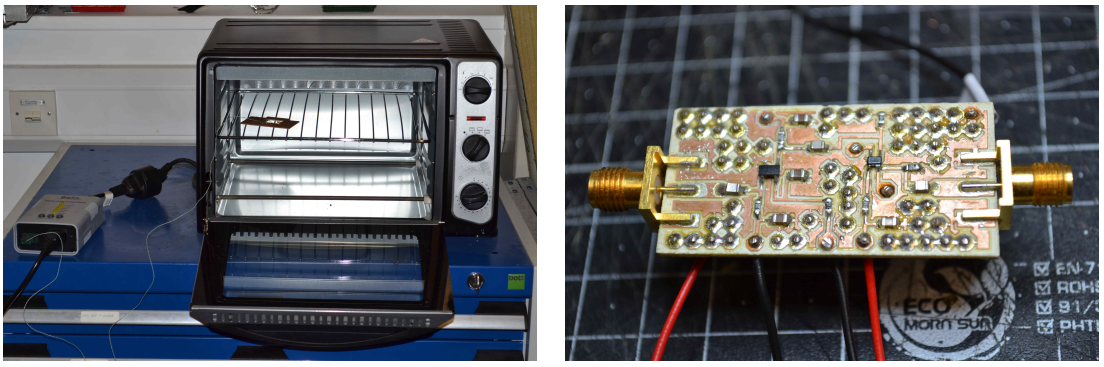
As well as the CNC router and electroplating, the group also has capabilities for a range of more common processes, which will be summarised in the list below.

- **Circuit Boards** The CNC router was equipped with a depth controller device, which facilitated the cutting of circuit board tracks for both rapid prototyping and final production. In addition to this, common tungsten carbide tools with appropriate cutting geometry will cut the low-loss glass fibre boards just like any other material, which gave us the ability to cut boards to any arbitrary shape, as well as the ability to drill hole arrays, slots or pockets, which would otherwise have to be separate processes in a 'wet' production set up - without the need for solvents, masks, photo-resists etc. This meant boards were not limited by shape and could by made to be complex shapes, which is useful for fitting into the tight spaces in the cryo-system. These features allowed circuits to be quickly designed, cut and ready for soldering and installation.

- **Batch/Bulk Soldering** Surface mount components are notoriously tricky to solder by hand with an iron, and while it is not impossible, a few systems were used to make the process quicker and easier. For small batches a butane heat pen can be used. This is nothing more than a butane torch combined with a catalyst to create hot air. One problem with this is it lacks real temperature control, risking component damage when working with temperature sensitive pieces. The heat pen is very useful for component removal, as it can apply heat over an area, allowing it to reflow many solder joints at once. Also useful for this is a 1800W electric

heat-gun - more commonly used for stripping paint and other DIY tasks - but provides exceptional large area heating for when whole boards need stripping, for recycling etc.

For more involved tasks such as amplifier and filter board manufacture, when there are many solder joints to make, a reflow oven was purchased from *BETA layout*, consisting of a simple oven and temperature controller set-up. The temperature profile is controlled with a control unit which 'learns' the heating profile of the oven, and adjusts the ramping rate accordingly. This allows consistent solder results, and prevents the oven heating too quickly or overheating and damaging components. A picture of the set up is shown in 5.16(a), as well as a multi-component board soldered by this method, shown in 5.16(b).

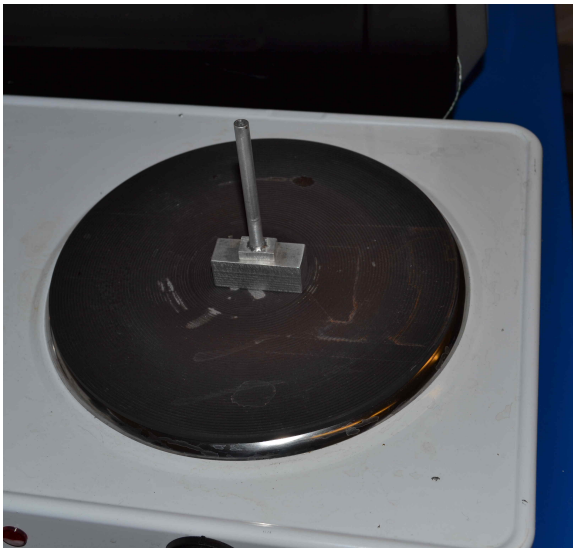


(a) (b)

FIGURE 5.16: The reflow oven and controller are shown in figure 5.16(a), the controller unit is shown to the left of the oven. This device regulates power available for the oven to use, in accordance with a pre-saved temperature profile, to ensure consistent results. An example of a board produced is shown in 5.16(b).

In addition to the reflow oven, a hotplate proved invaluable for the soldering of pieces with a large thermal mass, for example blocks of aluminium. The plate gave very even heating compared to an iron, and applies the heat quicker than the reflow oven, reducing metal oxidation. Aluminium is difficult to solder for the same reason it is difficult to plate, namely the oxide layer, so a specialised solder was necessary as it contains a suitable flux to facilitate soldering. The solder alloy used was *Alusol 45D* wire - a mix of lead, tin and silver with a water-soluble flux core. The joint was vacuum tight (tested down to $\simeq 10^{-8}$mbar), and used for bonding thin pieces of aluminium or copper, where any attempt to weld would melt and damage the surrounding area due to the low melting temperature of

the aluminium. An example of the plate and resulting joint are shown in figures 5.17(a) and 5.17(b).



(a)

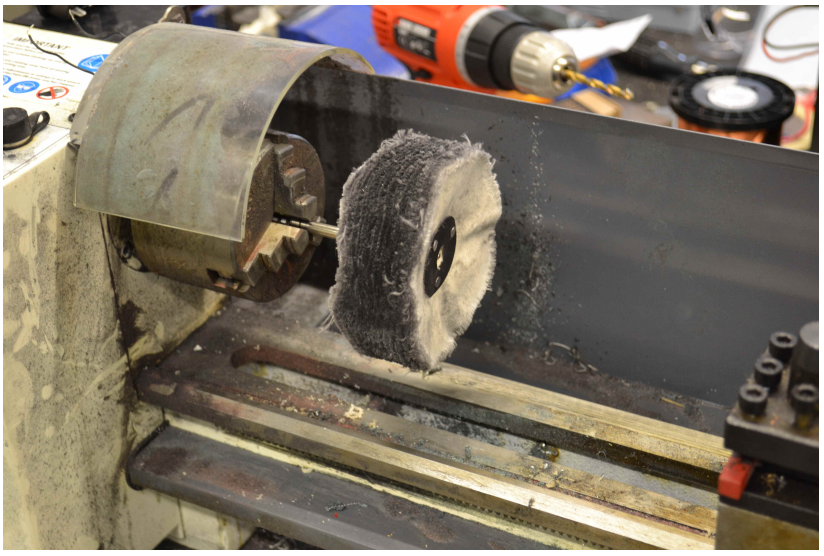
(b)

FIGURE 5.17: The hotplate used for soldering aluminium is shown in 5.17(a), and the resultant joint is shown in 5.17(b).

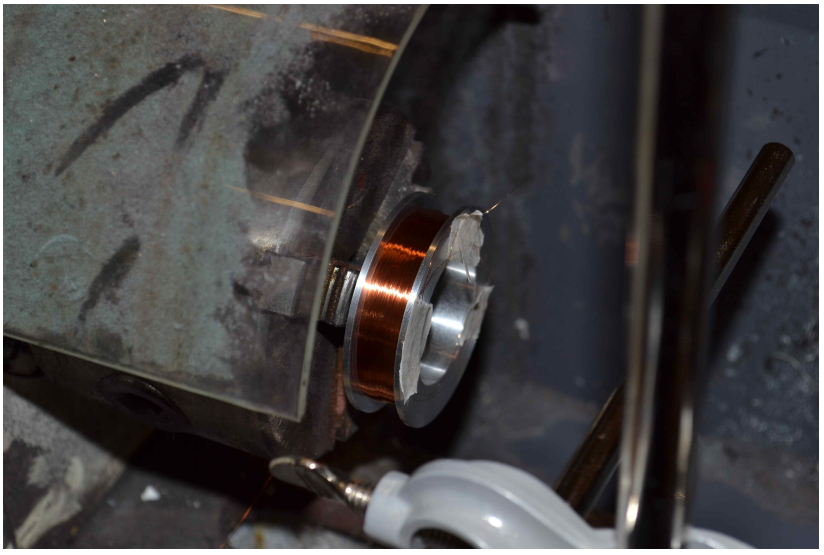
- **Lathing** A small lathe was purchased to work components with radial symmetry, such as tubes, screws and PEEK plastic bushings. However the main use of the lathe is for the next two points.

- **Coil Winding** With the addition of a magnetically triggered counter, and a felt pad tensioning system, the lathe functions as an effective coil winder, able to wind at 2500 turns per minute.

- **Polishing** Use of a various buffing wheels and compounds with the lathe can give mirror shine results of almost any material, included plated materials. Using suitable wheels it can be used to remove oxides, burrs, and polish all common metals such as steels, aluminium, copper and has been used to polish the niobium resonator.



(a)



(b)

FIGURE 5.18: The lathe was most used for the purpose of polishing, shown in 5.18(a), and also - with the addition of a magnetic switch linked to a rotation counter - for winding coils 5.18(b), as well as being a useful machine tool in its own right.

Chapter 6

Electronic Detection and Refrigeration

6.1 Detection Principle

The theory of the electronic detection of a charged particle in a Penning trap is discussed in section 2.2.5. A more technical summary is as follows. The signal chain starts with the image currents induced in the electrodes used to confine the particle. A stationary charge held close to a conductive surface is balanced by an appropriate deflection of charge density in surrounding conductors, giving the appearance of positive mirror charges, acting on the same principles as you could expect to find in a capacitor or similar arrangement, and as such, a particle in a Penning trap has an associated capacitance (figure 6.1). As the particle undergoes motion, these mirror image charges also undergo motion at the same frequency, giving rise to AC image currents on the surface of the electrodes, which in turn can be used to view the particle [114]. In the case of the singly-charged electron, these currents are of the order of femptoamperes, and so it is necessary to amplify this signal multiple times before it can be observed or recorded in the laboratory. A simple way to do this is to use an LC tank-circuit, tuned to have resonance at the motional frequency [63]. This circuit consists of an inductor surrounded by grounded shielding. The parasitic self-capacitance of the inductive coil appears in parallel with the inductor, forming an LC resonator. This can then be arranged between signal-line and ground, such that it presents to the particle a very high impedance

Z_ω at the resonant frequency. As the system has a base-level of thermal voltage and current noise, the resonant voltage profile can then be detected by a suitably sensitive amplifier, and displayed on a spectrum analyser. Since the electron itself has an effective capacitance and inductance, these act to 'short out' the resonant peak of the thermal spectrum, leading to the particle's 'noise dip' [63].

6.2 Axial Detection

The axial detection is performed by a resonant LC 'tank circuit, tuned to give maximum impedance at the axial frequency ω_z. When driven by the thermal Johnson noise generated by the system temperature of 4K, this impedance gives a Lorentzian voltage profile which is fed into the first amplification stage. The Q factor of which is determined by losses in the system, e.g resistive or dielectric losses in the resonator system. Discussed in section 2.2.8, the Q-factor must be maximised in order to have maximum visibility of the particle.

6.2.1 Axial Noise Dip

The presence of particles in the trap is detected as a 'dip' in the impedance profile of the resonator. This occurs because the particle shorts across the coil. The relationship can be thought of as two LC circuits [63]. The helical resonator appears as an inductance L_{coil} and capacitor C_{coil} in parallel between signal and ground, creating an impedance maximum. The particle appears in the opposite configuration (shown in figure 6.1), with an inductor L_{electron} and capacitance C_{electron} in series, which creates an impedance minimum, shorting out the signal at the frequency ω_z. A simulation of this response is shown in figure 6.2.

6.2.2 Axial Effective Coupling Distance

A mathematical description of the effective coupling distance is found in section 2.2.7. The effective coupling distance is crucial for determining the interaction strength between the electron and the detector system. As stated in equation 2.33, the effective coupling distance for a given electrode Σ, is equal to the normalized electric field at the

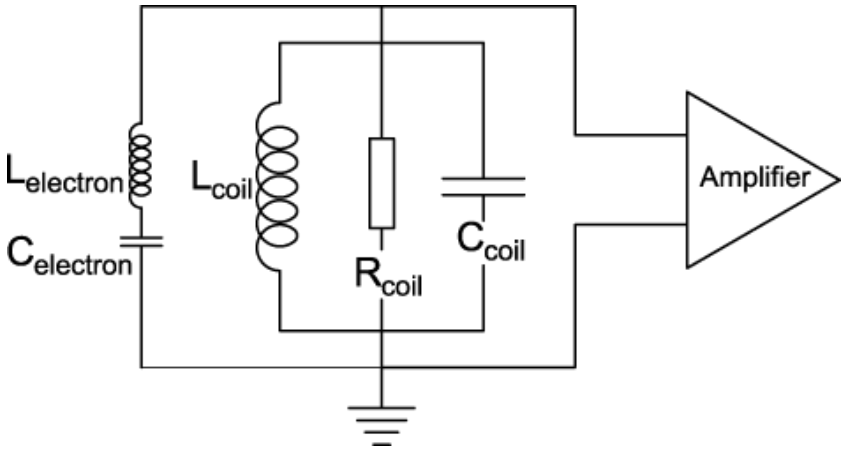


FIGURE 6.1: The equivalent circuit of the electron and tank circuit combined.

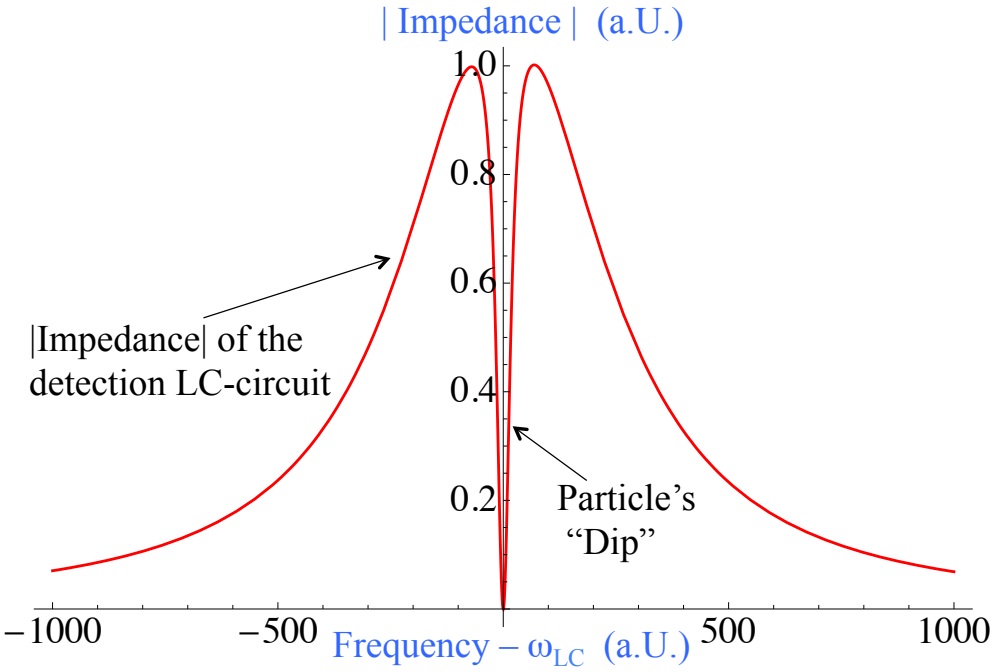


FIGURE 6.2: A simulation of the expected detection spectrum of the particle and resonator. The impedance of the system drops sharply at the frequency ω_z, as the particle acts as an AC-short to ground at this frequency. The interaction creates the axial 'dip' shown.

position of the electron i.e. $\vec{D}_{\text{eff}}^{-1}(y_0;\Sigma) = \frac{1}{1\text{ volt}}\vec{E}_\Sigma(0,y_0,0)$, and is thus related through the electron charge to the cooling force exuded on the electron, equation 2.30, which slows its motional velocity and hence cools the particle. The symmetry of the chip about $z = 0$ means that the physically closest electrode to the trapping position (the ring electrode) has no axial interaction with the detection system through this electrode, having an effective distance $D_z^{\text{eff}} \to \infty$, the same is true for the two side ground plane electrodes. This means that no cooling or detection can be performed through these z-symmetric

electrodes, and must instead be performed through one of the electrodes not symmetrical about $z = 0$, either a correction electrode or an end-cap. The effective coupling distance is strongly related to the strength of the electric field, and so as the strongest possible interaction between electron and detector is desired, of these two choices the correction electrodes are designated as 'pickup electrodes' due to their closer proximity. A full mathematical description of the Geonium Chip effective coupling distances can be found in [60].

6.3 Cooling the Axial Mode

The primary method of cooling the Axial mode is by the method of resistive cooling, whereby the electron is coupled to an electrical system, in this case the 'tank' circuit. Energy is exchanged between the resonant circuit and the trapped electron, until thermal equilibrium is reached with the surrounding system at 4.2K. When this state is reached, the total energy of RF photons radiated by the electron is equal to the number received from the blackbody radiation of the surrounding system. As the electron is coupled to the electronic system, any electronic noise - whether externally generated or internally e.g. Johnson noise - manifests as temperature at the electron, as the particle 'sees' the detection system as a temperature bath. Thus care must be taken with the amplifier circuitry to avoid sources of noise - which effectively heat the electron.

6.4 Amplifiers

The signal requires a number of amplification stages before it is able to be displayed for measurement. As each one of these stages could potentially be a source of noise, or otherwise distort the signal reducing measurement accuracy, they need to be planned carefully. This is most crucial in the initial stages of amplification closest to the measurement source, as any noise added will be amplified by subsequent stages, and the signal to noise ratio can quickly become unacceptable. For this reason, the first stage of amplification takes place as close to the trapped electron as possible, in the cryogenic section of the apparatus, where the Johnson noise is lowest.

The amplifier was a straightforward two stage set up, with one gain stage and one voltage buffer stage, for transforming the high output impedance of the gain stage, to the 50Ω coaxial line. The design of this amplifier was made easier as the axial frequency range of ≈25-30MHz is approximately the same as the cyclotron frequency of some proton Penning trap experiments, and thus the detection circuitry described in [91] could be easily adapted. The gain stage takes the form of a dual-gate GaAs transistor, and is arranged in common-source configuration for maximum voltage gain. The dual gate transistor can be compared to a 'cascoded' pair of single gate transistors housed in the same package, with the second transistor in common-gate configuration, as shown in figure 6.4. The main benefit of this is a reduced 'Miller Capacitance', which is the parasitic coupling between the input gate 1, and the output at the drain. In a single transistor in common-source arrangement, the Miller effect appears as negative feedback from the drain into the gate input. This is because the common-source amplifier is 'inverting' i.e. a positive voltage swing at the gate causes a negative swing at the drain, and thus any backwards coupling to the gate subtracts from the input signal. This serves to reduce gain, and is dependent on frequency, causing the high frequency cut-off to be lower than it should otherwise be for a given transistor. If the current path to ground is considered, the Miller capacitance has the same effect as a bleed-off capacitor between input and ground, increasing the input capacitance, and reducing the input impedance of the amplifier [115]. The value of this Miller capacitance C_{Miller} is a function of the voltage gain A_V, and the frequency independent gate-drain capacitance C_{GD}: $C_{\text{Miller}} = C_{\text{GD}} \cdot (1 + A_V)$. For example, a transistor gain of $20dB$ would scale any C_{GD} to 1+100=101 times its previous value, serving to add a capacitance of several hundred picofarads. A cascode arrangement shown in figure 6.4(b) drastically reduces the Miller effect by allowing drain-source current I_{DS} to flow through the transistor(s), with greatly reduced voltage swing at the drain of transistor 1 (D_1), as the impedance of transistor 2 is low, thus the voltage gain of $T1$ is low. The voltage swing still occurs as the current I_{DS} is still flowing through the load resistor R_L, but at the drain of transistor 2 (D_2). As transistor 2 is in common gate configuration, it is not susceptible to the Miller effect, as the gate shields the drain signal from feeding back into the source, so this means the gain of the amp no longer scales the feedback capacitance, and hence it is greatly reduced.

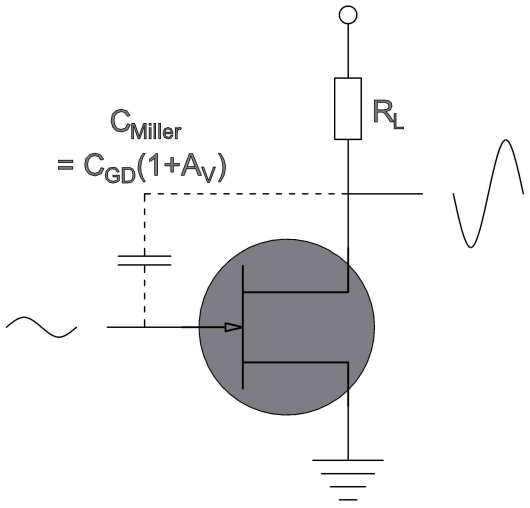


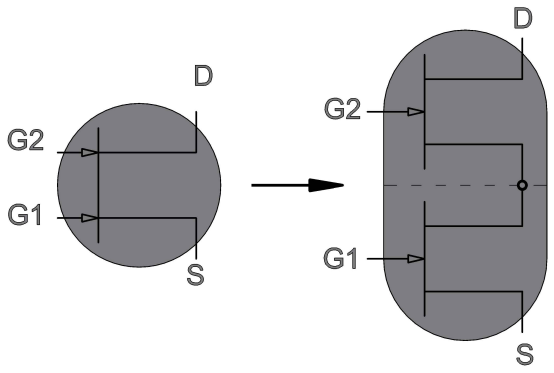
FIGURE 6.3: Sketch of a common-source amplifier layout, with the Miller capacitance marked. (Appropriate biasing is assumed). The capacitance couples the inverted output signal at the drain, to the input signal at the gate. This serves to reduce the input seen at the gate and hence gain. Coupling strength increases with frequency.

A gallium arsenide transistor was chosen as it is a tried and tested cryogenic semiconductor [94], with a history of success with low-noise Penning trap experiments due to its low noise characteristics, frequency performance and semiconductor band-gap allowing for cryogenic use. However, as of writing this thesis, the technology is becoming outdated, and components are increasingly hard to source. It may be necessary in future experiments to find cryogenic compatible devices which make use of a different semiconductor for example PHEMT devices [116].

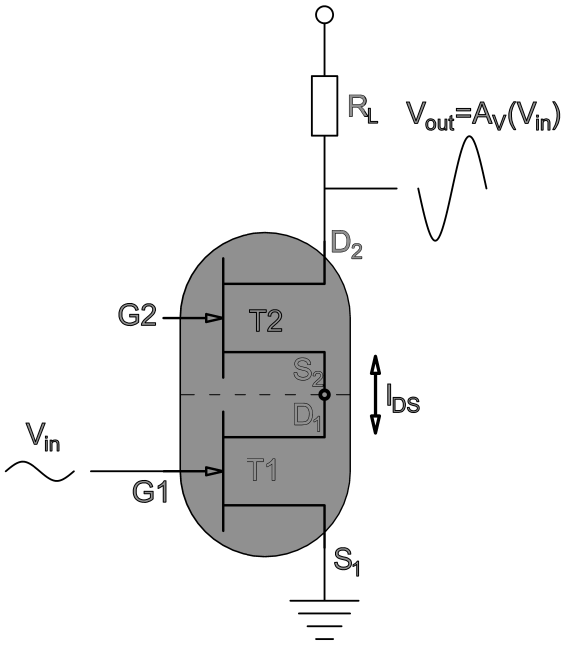
To summarise, the importance of the feedback capacitance is that is serves to reduce the input impedance of the amplifier, and so in order to avoid degrading the Q-factor of the resonant tank circuit at the amplifier input, it must be minimised [87, 115, 117]. The input of a dual-gate (or cascode) circuit is high, and retains the high gain of a common source design, without suffering the effects of a high Miller capacitance that a single gate common-source amplifier is subject to.

6.5 Experimental Realisation

The electronic detection system needed to be built from scratch, and the following section details some of the progress made towards an effective detection system. As the



(a)



(b)

FIGURE 6.4: Equivalence of the dual-gate transistor to two single gate devices. The benefits of this include reduced gate-drain capacitance (Miller capacitance)

cyclotron mode is beyond the scope of this thesis, only the axial detection circuitry will be discussed here. General rules for RF circuitry were followed, including

- The use of surface mount components is essential if parasitic effects are to be minimised. Above the MHz range, through-hole components are less well suited due to the long wires and comparatively bulky packaging, which give rise to parasitic

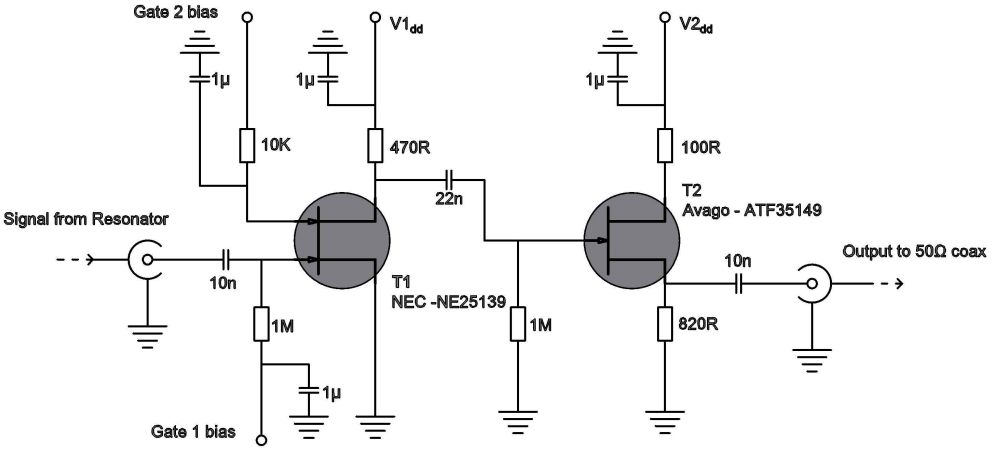


FIGURE 6.5: Circuit diagram for the amplifier.

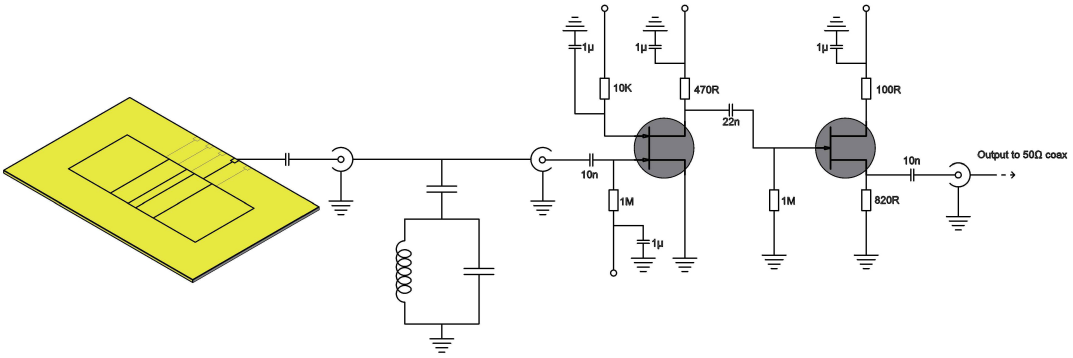


FIGURE 6.6: A diagram of the Geonium Chip detection wiring

capacitances and inductances which can cause instability through feedback, and degrade the detection Q-factor.

- The use of low-loss circuit board is essential, so high-frequency boards (*Rogers RO4000 series*) were used throughout the wiring.

- Good quality, low-noise components were used, including coaxial cables, connectors, thin-film resistors and high-Q capacitors.

- Wire lengths were kept to a minimum, and shielded wire was used wherever possible. This not only reduces signal attenuation, but reduces cross-talk and interference between signal paths. For opposing signals, such as current carrying wires, twisted pairs were used to cancel out noise.

- A well defined ground plane is essential for reducing noise and inter-board capacitances. For this reason, many vias were made between the cladding of the boards

(this was made simple by the CNC mill and bulk soldering processes detailed in section 5.4)

A diagram of the axial signal chain is shown in figure 6.7. The resonator and pre-amplifier are positioned as close as possible to the point of detection. After the signal is generated as a voltage across the resonator, it passes through a number of amplification and filtering stages at each thermal stage, in order to maximise the signal to noise ratio. Depending on the final Q-factor of the coil and detection system, the width of the axial dip could be as low as a few tens of hertz, and so a high resolution HP35670A FFT dynamic spectrum analyser is used as it has a resolution in the micro-hertz range. The analyser has a frequency range of up to 102.4kHz, and thus the axial signal must be down-converted from ν_z to within this range, by mixing the detection signal with a high stability sine wave ν_{fgen} from a frequency generator. When mixed with ν_{fgen}, the new signal has side bands of $\nu_{\text{signal}} \pm \nu_{\text{fgen}}$, thus if a suitable frequency of ν_{fgen} is chosen,so that $\nu_z - \nu_{\text{FFT range}} < \nu_{\text{fgen}} < \nu_z + \nu_{\text{FFT range}}$, the axial dip can be observed on the FFT to high resolution.

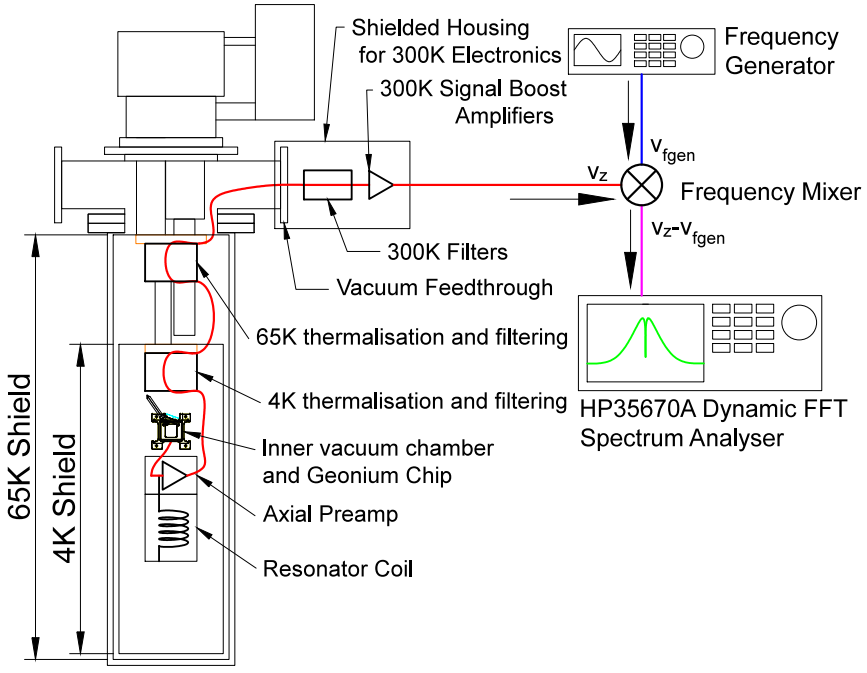


FIGURE 6.7: Shown is a block diagram of the axial signal chain. After detection, the axial signal chain passes through a number of amplification stages, as well filter stages to remove anything other than the signal of interest, before being down-converted for display on the FFT analyser.

6.5.1 Resonators

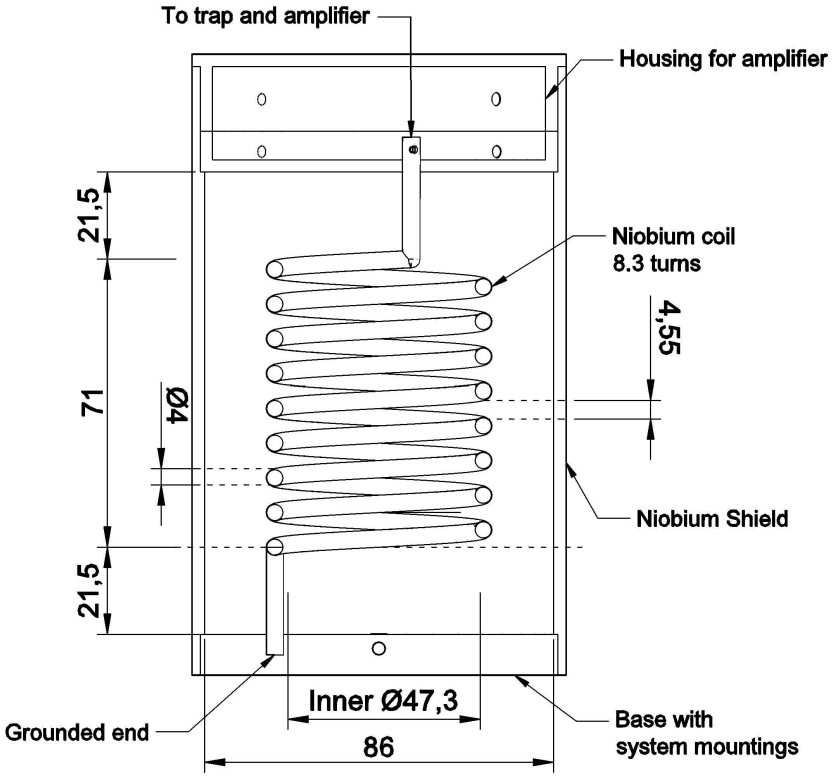
As each frequency of interest lies in different regions of the frequency spectrum, it is necessary to have two separate tuned resonators, one tuned to match the radio frequency of the axial mode ω_z and another entirely separate resonator for the microwave frequency cyclotron mode ω_+.

The axial resonator uses the well known cylindrical helical resonator, designed along principles commonly used radio frequency communications [118]. As it is away from any magnetic field (as a result of not using a large-bore solenoid magnet), it was decided to construct the resonator from pure niobium metal, which is a type II superconductor when cooled to below its critical temperature of 9.3K [98]. It is important to note that this material choice would not be usable in the more common large bore solenoid Penning set up, due to the relatively low critical field of pure niobium[119], however in low fields, the residual surface resistance of pure Nb is 5-20 times smaller than NbTi and should lead to higher Q-factors when optimised [64, 120].

The Q factor of a helical resonator increases with increased diameter, so the resonator cylinder was chosen to be the largest diameter allowable in our system. A large diameter cylinder also means that the central inductor can be made large, allowing it to hold its shape without the need for a support core, which eliminates the possibility of any such core contributing dielectric losses to the system and degrading the Q-factor.

The coil is designed along guidelines detailed in [118].

(a) (b)



(c)

FIGURE 6.8: 6.8(a) shows the niobium coil and shield, before polishing, and after polishing is shown in figure 6.8(b). The coil is made from 4mm diameter niobium wire, and is able to support itself without the use of a core. The dimensions of the coil are shown in 6.8(c).

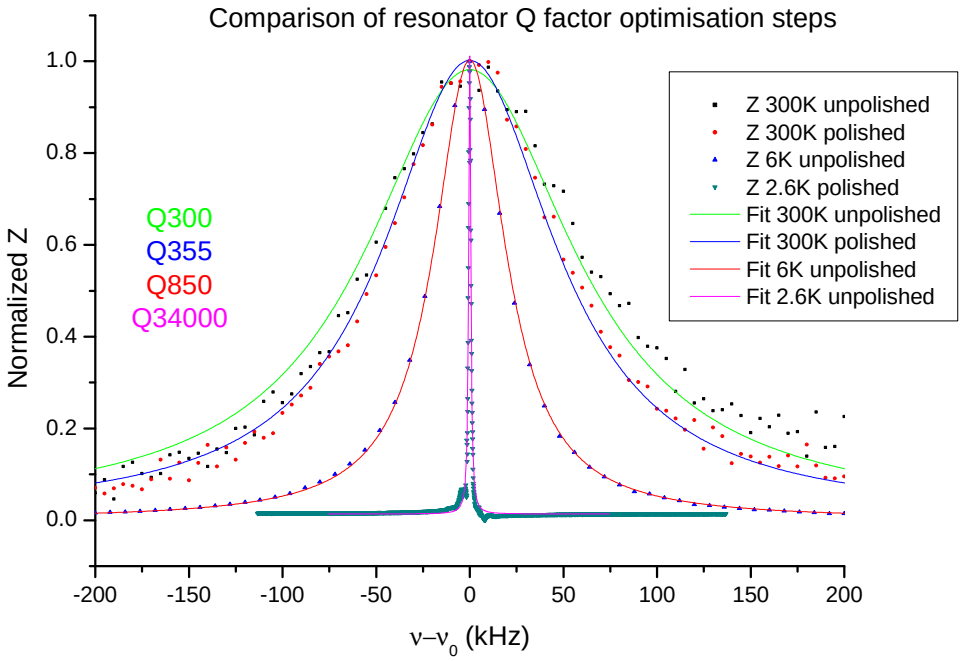


FIGURE 6.9: A comparison of the effect of temperature and polishing on the unloaded Q-factor of the coil is shown. At room temperature, polishing of the coil yields a modest Q improvement of 18%. This improves significantly when cooled to cryogenic temperatures*, and improved by two orders of magnitude when mechanically polished and cooled below the critical temperature T_c. *The characterisation of the coil was subject to a number of thermalisation problems with the pulse-tube system, and so did not reach the desired temperature of <4K for the unpolished measurement. The issues were resolved by the time resonator had been polished, hence the difference in cryogenic temperatures.

Polishing the coil had the effect of raising the room temperature Q-factor by 18% from 300 to 355. As polishing reduces the effective surface area, and hence surface resistance, the main benefit of the mechanical polishing can be seen at cryogenic temperatures. The thermalisation problems with the cryocooler mentioned in the caption were resolved, and a cryogenic Q-factor measurement is included in figure 6.9. When optimised as detailed in [64], the Q-factor of the coil was measured to be $\simeq 34,000$.

TABLE 6.1: Parameters of the axial resonator

	Value	Units
Unloaded ν_0	46.8	MHz
Unloaded Q at 300K	355	-
Unloaded Q at 2.6K	34000	-
Self-Capacitance	8.32	pF
Inductance	1.39	µH
Effective R_p at 2.6K	13.9	MΩ

Q-factor measurements were performed by weakly coupling the the coil through an air-core capacitor of approximately 0.3pF, and measuring the response on a *Keysight FieldFox 29923A* vector network analyser. Measuring the inductance L on a *ISO-TECH* LCR meter, the capacitance could then be extracted from the resonant frequency by the relation $C_{\text{coil}} = 1/\omega_0^2 \cdot L_{\text{coil}}$

6.5.2 Axial Amplifier

The amplifier needed to fulfil certain criteria. Specifically, it must have high input impedance to avoid loading the resonator and degrading the Q-factor, and low Miller capacitance for the same reason [115], while also having extremely low noise and function at cryogenic temperatures [94]. A gallium-arsenide FET has an extremely high input impedance, and functions well at cryogenic temperatures as the band-gap of GaAs is an order of magnitude lower than that of silicon, allowing for cryogenic use [93]. The miller capacitance can be addressed by using cascoded transistors, or for convenience a dual-gate device can be used as it is analogous to two cascoded transistors sharing a single substrate, detailed in section 6.4. Arranged in common source configuration, the device yields approximately 12dB gain at 30MHz.

To match the high output impedance of the amplification stage to the 50Ω of the coaxial cables, a 'source-follower' is used, to convert the signal from a voltage source to a current source [92].

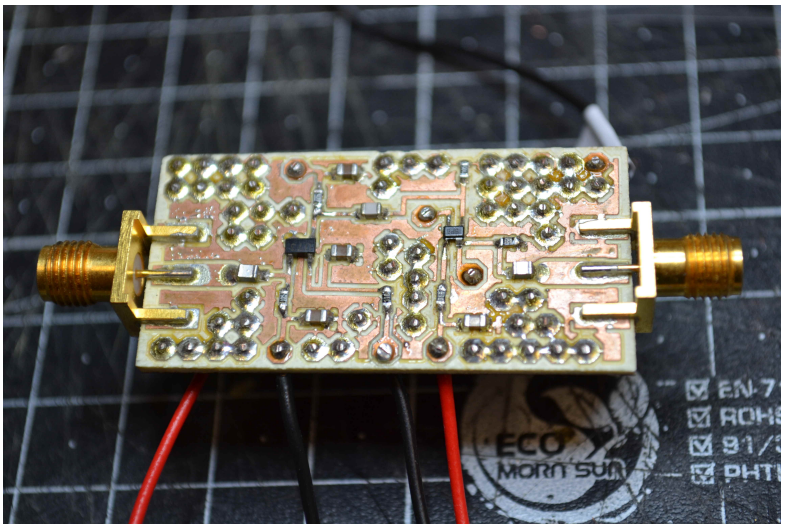


FIGURE 6.10: The axial amplifier is shown. The board was cut from double clad low-loss RO4000 series board on the CNC machine, which also facilitated the drilling of a pattern of vias, drilled in order to minimise the inter-board capacitance, which can degrade the performance of the amplifier. In operation, the amplifier is housed within the casing of the axial resonator.

6.6 Cyclotron Preparation

Observation of the cyclotron motion of a single electron in the Geonium Chip is a primary goal of the Geonium Chip. A sufficiently optimised system should be able to resolve the cyclotron frequency *directly*, without the need to measure through side-band coupling. This would be achieved by pushing the trap into the 'ultra-elliptical' regime discussed in section 2.2.4. This ultra-elliptical regime causes the magnetron motion of the electron to vanish, and the reduced cyclotron motion ω_+ goes to ω_c. Because the Geonium Chip is elliptical, and the electrodes are not symmetrical about y_0, the cyclotron frequency can be observed though the y component of its motion. For the first generation chip, the signal will be detected by a near-field coplanar wave-guide positioned under the chip. As the metallisation of the chip is thin enough - many times thinner than the skin depth - such that the cyclotron signal will not be completely reflected by the surface, and will instead be transmitted through, allowing AC MW coupling, without modifying the potential landscape of the trap. The preparation and initial measurements of this effect are detailed in section 6.6.3

6.6.1 Cyclotron Amplifier

Although the cyclotron amplifier will be a crucial part of the fully functioning Geonium Chip, it is beyond the scope of this thesis, as time restrictions limited their development. It is however possible to predict certain characteristics of the device, as it will likely be constructed along the lines of gigahertz frequency technologies used in wireless communications, such as MMIC construction methods. Thus gigahertz frequency technology is becoming more commonplace and should follow standard MW communications guidelines. Low noise, low temperature devices have applications in the field of satellite communications and as such literature is available to realise the detection circuitry of the cyclotron motion. The cyclotron signal will undergo a similar pre-amplification stage - induced signal, high impedance resonator, low noise amplifier etc. - but the frequency regime means that the component and circuit design will have to be approached in a different way. Due to the shorter wavelengths, the cyclotron resonator could be constructed from a waveguide-cavity, of the type demonstrated to have Q factors of $\simeq 10^5 - 10^6$ by using superconducting materials and micro-fabrication techniques [52, 121–123]

6.6.2 Microwave Screening Chamber

The 'microwave screening box' enveloping the trap is designed to suppress spontaneous emission and absorption of microwave frequency photons. With the goal of exploiting the 'Purcell effect' [124], the box forms a MW cavity, with the resonant modes far off-resonant to the cyclotron mode ω_+ of the electron. This means that the range of frequencies that is supported by the trapping volume is reduced to a finite number of discreet modes. This reduces the probability of a photon with frequency ν_+ being released into the enclosed space, as its mode would not be supported in the cavity, and thus it acts as a spatial filter. The solutions to this problem allow flexibility as there are a great number of length, width and height combinations which will satisfy these off-resonant criteria. Thus the scalability of the chip is not hindered by the cavity, as the box can be made larger or smaller to suit, perhaps enclosing many multiples of the chip trap.

The screening chamber is a cube of side length 20mm, with the bottom face comprising of the chip surface, centred on the coordinate (0,0,0). For the target B_z of 0.5T, at the corresponding ω_+ of $2\pi \cdot 13.99$GHz, has a nearest resonance 910 MHz away at 14.9GHz.

6.6.3 Through Chip Signal Transmission

The nature of gigahertz frequency radiation allowed a novel trick to be used for interacting with the electron's cyclotron mode. Since the addition of high frequency cabling such as coax or waveguide would complicate the trapping space and introduce undesirable dielectric material close to the trapped electron, the decision was made to exploit the skin depth δ of GHz frequencies in metals, the value of δ is dependent on bulk resistivity ρ of the metal and the frequency of the wave f [83]. This way, no dielectric is visible, and there is no distortion to the DC electrostatic potential. If the metal is sufficiently thin, the microwave will pass through, suffering an attenuation exponentially proportional to the thickness, and the skin depth δ at that frequency.

$$\delta = \sqrt{\frac{2\rho}{(2\pi f)\mu_R \mu_0}} \tag{6.1}$$

This depth is described as the distance in m required for a wave travelling in a given medium to drop to $1/e$ of its initial amplitude. The current density J is linked directly to the electric field radiated on the transmission side, and so transmission through the metal layer of thickness d can be calculated to be

$$J = J_0 e^{-\frac{d}{\delta}} \tag{6.2}$$

and so when $d = \delta$

$$\frac{J}{J_0} = e^{-\frac{\delta}{\delta}} = 1/e \tag{6.3}$$

The basic set-up for testing transmission through the chip is shown in figure 6.12(a) for room temperature. In the set up a coplanar wave-guide is placed under the chip, and terminated at one end with a short. An example of the results obtained can be seen in figure 6.11. The attenuation is related to the current density J and hence electric field strength on the surface of the chip closest to the detector. From the equations 6.1 and 6.2 it can be seen that as resistivity decreases, so does the skin depth δ, and hence a

thinner layer is required to see the same transmission amplitude. As the resistivity ρ varies with temperature, it was necessary to test transmission at various temperatures to gain an understanding of the mechanisms involved.

The resistivities and corresponding skin depths are tabled in 6.2

TABLE 6.2: Resistivities and the corresponding skin depths for Geonium Chip for the temperatures 300K and 4.2K, denoted by the sub-indices

Resistivities ρ ($\times 10^{-8}\Omega$m) and Skin Depth δ (nm) for Alloys and Metals Considered for the Geonium Chip at 14GHz				
Material	ρ_{300K}	δ_{300K}	$\rho_{4.2K}$	$\delta_{4.2K}$
Pure Gold	2.271	641	0.022	63
Pure Silver	1.629	543	0.001	13.5
Alloy 50Au50Ag	10.42	1373	8.37	1231
Alloy 80Au20Ag	9.55	1314	7.3	1149

The first generation Geonium Chip has been manufactured with 3 different metallisation layers, and their expected transmissions J/J_0 are listed in table 6.3.

TABLE 6.3: Expected transmission through the Geonium Chip

Percentage Transmission $J/J_0 \cdot 100$ for the specific depths d and alloys of the Geonium Chip at 14GHz		
Material	300K	4.2K
Pure Gold $d = 300$nm	62.6%	0.85%
80Au20Ag $d = 300$nm	79.6%	77.0%
80Au20Ag $d = 100$nm	92.7%	91.7%

Example results from a through-chip scan can be seen in figure 6.11, and a room temperature and cryogenic scan can be seen in figures 6.12(a) and 6.12(b) respectively. When taking into account a reflection coefficient of 0.55 for the air-silicon-metal interface, the transmission agrees with theory to within 5% for 80Au20Ag alloy.

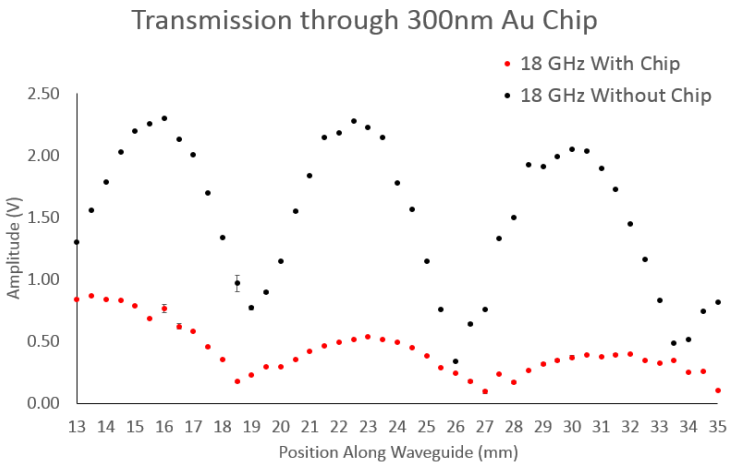
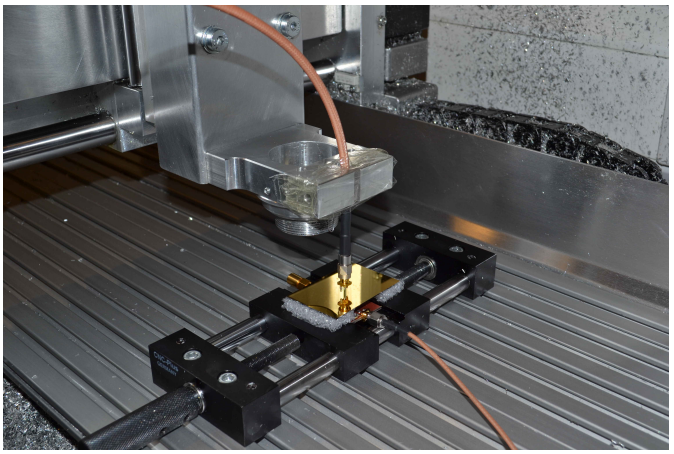
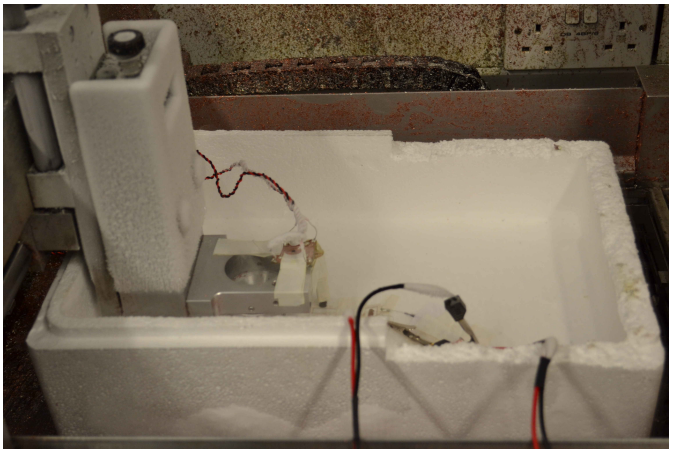


FIGURE 6.11: An example of the attenuation observed can be seen, in this example the chip used had a metallisation of 300nm pure gold on 1mm of silicon. Though suffering an attenuation, the standing wave pattern is clearly seen (*results taken by John Lacy of the Geonium group*).



(a)



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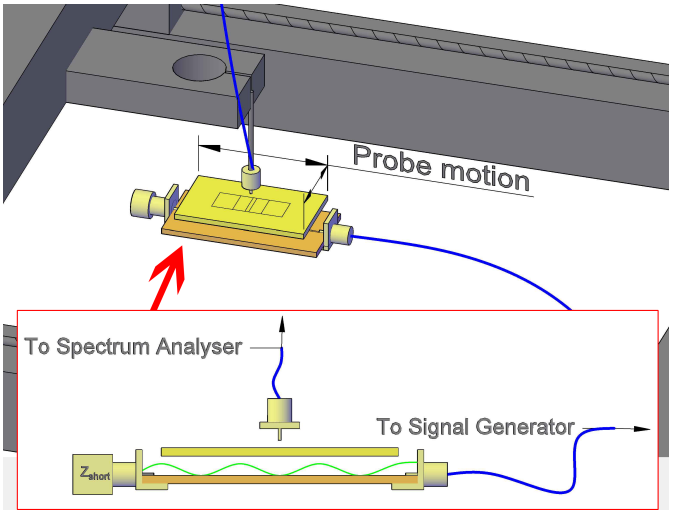


(c)

FIGURE 6.12: Some example pictures of the test set up used to measure transmission through the chip surface. The room temperature measurement is shown in 6.12(a). Under the chip, a short section of terminated coplanar wave-guide has a standing wave set up upon it, at the frequency range of interest, sketched in figure 6.12(c). A coaxial cable with a short aerial is attached to the armature of the CNC machine, and used as the pickup. The coax is attached to a spectrum analyser, and the detected amplitudes were outputted to a computer where it is combined with the corresponding CNC coordinate. A similar method was employed when measuring at liquid nitrogen temperatures to test the effect of cryogenic temperatures. Figure 6.12(b) shows the system modified to hold a reservoir of liquid nitrogen.

Chapter 7

The Prototype Magnetic Field Source

7.1 Initial Magnetic Field Generation

The end vision of the Geonium Chip includes a compact magnetic source, which matches the scalability of the Geonium Chip design, and, in future generations of the chip will eventually become part of the microfabrication [66], for a truly compact device. The ideal system has perfect magnetic stability in time, with superconducting magnetic sources operating in persistent current mode with no loss. This section aims to outline the steps taken towards a first prototype, and a series of progressions planned to be taken in the near future to improve the design.

7.1.1 First Generation Planar Magnetic Field Source

The first generation of planar magnetic field source will be a centimetre scale, wire-wound array of coils wound with 0.4mm diameter NbTi copper stabilised wire, with a copper to superconductor ratio of 1.5:1, in other words, the superconductor occupies 40% of the conductor cross-section. The coils will be dimensioned appropriately in order to supply a homogeneous field of around 100 mT in the Geonium Chip trapping region, and in the process of doing so provide an experimental realisation of the coil theory outlined in section 2.4. The array will have discrete current sources for each pair of

coils, as this is the quickest and most reliable method for energising the coils. For this, a *Hameg HMP4040* supply will be used to supply the currents required. The stability of ±2mV is not good enough to achieve accurate measurements, but it is sufficient for preliminary testing. As stated earlier, maximum magnetic field stability is achieved, when the current is running in persistent, lossless loops. In a NbTi wire-based system, the problem of joining the superconductors without introducing resistance is presented, as any resistance would lead to an exponential decay in current flowing [125], as found in a standard RL circuit where R is the joint resistance and L is the inductance of the coil (equation 7.1). The joining techniques are discussed in section 7.3.7.

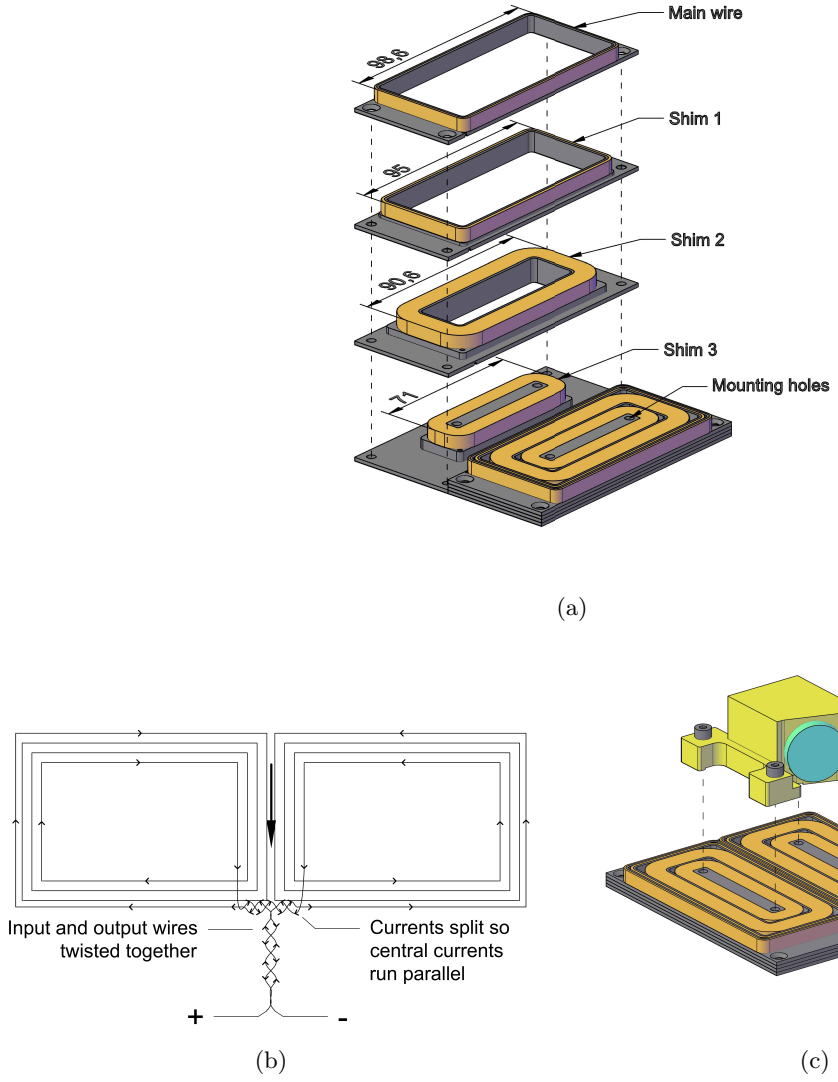
$$I = I_0 e^{-\frac{Rt}{L}} \tag{7.1}$$

TABLE 7.1: Wire cross-sections for the first prototype coil array

Coil	Cross Section ($w \times h$ in mm)
Main J_0	0.8×6
Shim 1 J_1	1.2×6
Shim 2 J_2	8.8×6
Shim 3 J_3	7.5×6

The wire is then wound onto spools and arranged into an array shown in figure 7.1(a). Rather than aligning the coil axes along z as would be found in Helmholtz coils, the spools are aligned along the y axis. This design imitates the field generated by a single current carrying wire. For this reason, rectangular spools are used, and the longest axis of the spools pass under the trapping region. In total, 4 pairs of rectangular coils are nested within each other, grouped into two lots of four concentric coils, and aligned with the y axis such that the inner wires of the coils pass under the trapping position as seen in figure 7.1(c), i.e. the coils are reflected about $z, x = 0$.

Since this first build is in essence rapid prototype, the cores are to be manufactured through the same processes detailed in chapter 5. The winding frame has been designed to be milled from single blocks of aluminium, and wound in-house, using 0.4mm superconducting wire previously obtained from *Supercon Inc.* To wind the coils, a lathe has



(a)

(b)

(c)

FIGURE 7.1: Figure 7.1(a) shows the basic assembly of the first generation wire-wound coils. They are designed to be wound in pairs. After each wind, the wiring is fed through to the back and then the next pair are added to the stack for winding, in the order of smallest (inner) to largest (outer). For simplicity, a diagram of the wiring is shown separately in figure 7.1(b). The wires are fed through holes/recesses to the back of the stack to the supply system. The coils share a common wire and hence have the same current flowing. Where possible, lengths of opposing current have been twisted together. In figure 7.1(c) the chamber with the Geonium Chip sealed in position is mounted directly onto the winding cores of the two coil stacks. The chamber and the stacks share a common 4mm screw to help align the chip with the currents flowing through the central region, where the two arrays meet.

been modified to include a magnetic switch and counter shown in figure 7.2, capable of rotation rates of up to 2500rpm. As the core is rotated, it draws the wire through two felt pads, which are in an adjustable clamp, in order to set even tension in the wire.

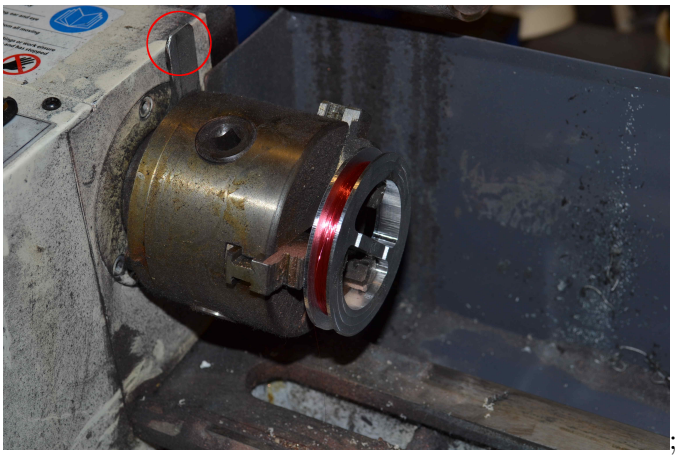

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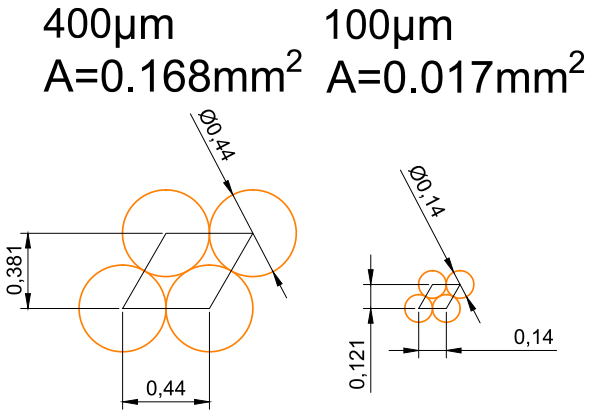
FIGURE 7.2: A test coil being wound with 56µm copper wire on the winding lathe. The lathe has been modified to incorporate a magnet (circled in red) which triggers a counter on each revolution, allowing for coils to be wound quickly and accurately. The tension is set by drawing the wire through two felt pads, adjusted with a screw clamp.

7.2 Thermal Load Considerations for Magnet Currents

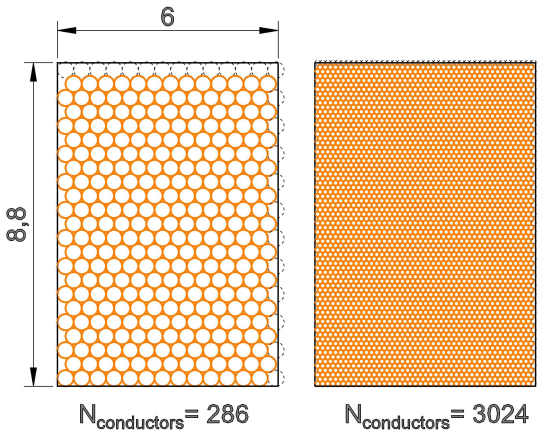
The comparatively large currents required for the magnetic system presented the problem of resistive heating in the sections of wire required to connect to the superconducting sections. In the rest of the system, the majority of the connections are low current, at most only drawing a few mA. This meant it was safe to use thin wires to minimise thermal conduction down the length of the wire. With higher currents, thicker wires must be used, and hence it is necessary to pick a wire diameter which minimises the *sum* of the thermal contributions from both the conduction down the wire, and the power loss from the wire using techniques found in [69, 89].

A simple way to reduce the current, and hence power dissipation at joints, in a superconducting coil is to use a superconducting wire with a thinner diameter (assuming the current does not exceed the critical current for the wire). Doing this allows for more wires per unit cross sectional area, and for a given current, the current density multiplies by the number of wires per unit area. For example, for the first prototype planar coils designed for the Geonium chip, the diameter of the wire is 0.4mm, clad in 0.02mm thick insulation, for a total diameter of 0.44mm. In close-packed arrangement as would be found in a cross-section of an infinite ideally wound coil, the area occupied by one conductor is 0.168mm^2 (shown in figure 7.3(a)). For a 0.1mm wire with the same insulation, the area occupied reduces to 0.017mm^2, allowing roughly 9.882 conductors to fit in the same area. In reality the wire cannot be subdivided and has to fit in in a finite spool,

but the decimal has been left as it becomes relevant in the case of large coils with many multiple thousands of turns. A comparison can be seen in figure 7.3.



(a)



(b)

FIGURE 7.3: A comparison of cross sectional packing of the 0.4mm diameter NbTi currently in use for the Geonium Chip magnetic prototypes, versus the 0.1mm diameter NbTi wire available. The ratio is not exactly 9.882 as the wire cannot be subdivided, and in this specific case it is actually higher at 10.573

7.3 Future Generation Planar Magnetic Field Sources

The first generation planar field source will be very basic, and is unlikely to have good field stability. This can be improved in a number of ways, including:

- Improving the current supply will yield better field stability, and devices are available which can supply extremely stable currents, with the only downside being the cost of the device.
- Improved winding density will yield higher coil inductance, which will help resist changes to the current, while at the same time reducing the amount of current required to achieve the same current densities, reducing thermal loads.
- Switched persistent mode operation would set up a persistent current, however, there is always some residual resistance at a joint, and a switched system requires at least one join to form a loop.
- Flux pumped persistent mode operation could be used on closed loops of HTS tape, and so the loss (and hence exponential decay) of the current is greatly reduced, provided the system is used at a low enough temperature to avoid significant flux-creep effects [126].
- Microfabrication techniques could allow a planar source to be manufactured inside future Geonium Chip substrates [66], completely eliminating any vibrational and alignment problems.

7.3.1 Superconducting Switches

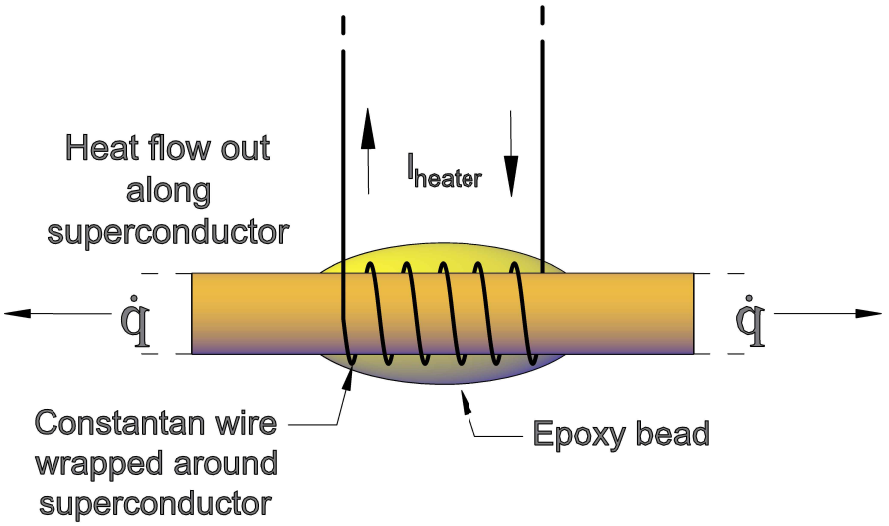
To generate the persistent currents in the coils, it is necessary to find a way to stimulate current in closed superconducting loops. As the flux-pump method is still under development at this stage, it was decided to build superconducting switches to allow use of a relatively inexpensive *HMP4040* current supply. As our current requirements are relatively small in the beginning i.e. < 10A for 50mT, this supply is sufficient and there was no need to use a more expensive dedicated superconducting magnet supply. Superconducting switches are routinely used in large superconducting solenoids, and consist of a way of locally breaking the superconductivity of a small section of the coil, while

current is applied, and then superconductivity is allowed to return - closing the loop. A schematic of this is shown in figure 7.5. Switching the wire is done by locally heating a small portion of around 4mm of the switch section NbTi wire above its T_c of around 9.3K[98], creating a section of non-zero resistivity. The current connections are made to either side of this heated region, and this forces the current into the coil loop. When the current is at the desired value and stable, the heater is turned off and the wire is allowed to return below its critical temperature, closing the coil loop into persistent mode, and the current supply can be switched off safely. The heaters are simply constantan alloy resistance wires, wrapped around the insulation of the NbTi wire and encased in a drop of cryogenic varnish or *Stycast* epoxy to fill any gaps between the heater and the NbTi and increase thermal contact. The heating wire used is 0.1mm in diameter, and has a rated resistance of 62.4Ω per metre, and is insulated from itself by an oxide barrier layer. The length of the resistance wire should be kept to a minimum to avoid unnecessary heat load upon the system.

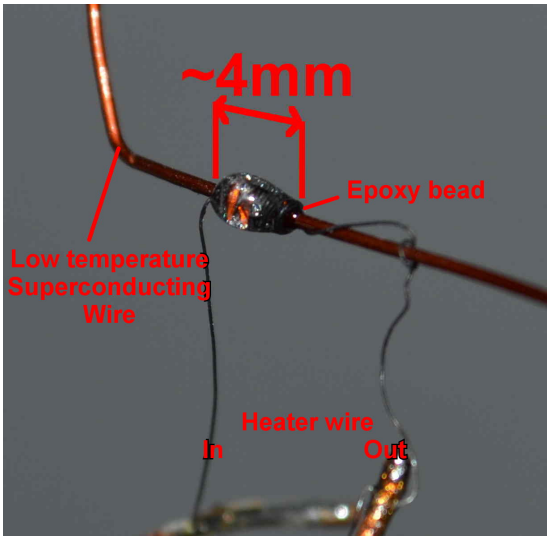
Heat loss and thus the amount of current required to hold the switch in the 'open' position can be assumed to be the sum of the two conduction paths along both sections of the wire from the heater to the thermal bath. In order to maintain a steady state 'open' condition at a given temperature, i.e. $T > T_c$, the power dissipated by the heater must equal the conduction away from the heated region. As the heat dissipation of the resistance wire is ohmic, it is sufficient to say that

$$I^2_{\text{heater}} R = 2 \times \dot{q} = 2\frac{\kappa A(T_c - T_{\text{bath}})}{l} \tag{7.2}$$

If the NbTi wire is approximated to be a 0.4mm diameter cylinder of solid copper, with thermal conductivity $\kappa = 1000\text{W/m·K}$ [89], attached at both ends to a 4K bath by a 50mm length of wire, then this gives a current of 70mA necessary to keep the switch in a steady-state 'open' of 10K (assuming 6Ω of resistance wire), and loading the system with approximately 30mW per switch.



(a)



(b)

FIGURE 7.4: A heating wire bonded to a section of NbTi wire. The wire is encased in cryogenic varnish or epoxy to give better contact with the wire.

7.3.2 Low Temperature Superconducting Wire

It was decided to use the well-known Niobium-Titanium alloy as the superconductor used in the 4K sections. This was because it is metallic rather than ceramic or inter-metallic, meaning it can be drawn into thin wires, is highly ductile, flexible, and allows for a very small bend radius - necessary for the rectangular coils. Intermetallic-based

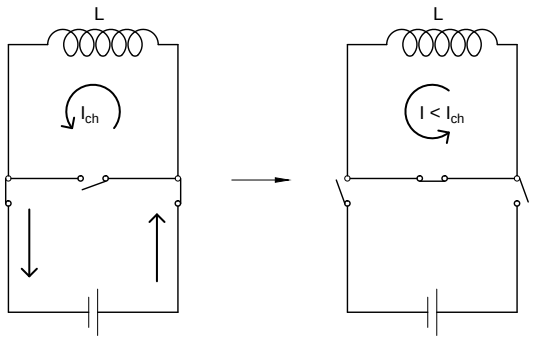


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FIGURE 7.5: With the switch open, the coil is charged with a current I_{ch}. When the switches are flipped, a small amount of inductive energy is transferred to the switch region, and so the remaining persistent current is less than the charging current, which must be accounted for when charging the coil [19].

low T_c superconductors such as Nb_3Sn have superior field characteristics, but are more brittle and can have continuity problems when subjected to sharp bends [98]. The wire chosen was *T48B-M*, comprising of a single 250µm NbTi core with copper cladding, giving a total of 0.44mm including insulation, purchased from *SuperCon*. Using a low-temperature superconductor requires less heating in order to trigger a quench, as the critical temperature is just a few degrees above the system level (The T_c of NbTi is approximately 9 kelvin). This means that more care must be taken at the low-temperature to thermalise wires, and make joint contacts as low-resistance as possible (details below in section 7.3.3).

7.3.3 Low Temperature Superconductor joints

Joining the NbTi to copper wires, for example the solder tags used to connect to the thermalisation blocks, is relatively simple as the NbTi is clad in electronic copper, so conventional soldering techniques can be easily employed. Once soldered to the solder tags, the tags are screwed to bus-bars in thermal contact with the cold-head. The joints between the NbTi wire and the tag are 45mm in length, with a width of 3mm. The joint area is limited by the surface area of the NbTi/copper wire, so to increase the length and hence area in contact with the tag, the wire can be soldered in a zig-zag path, or

wrapped around the tag and soldered on both sides. When a low resistance joint between two pieces of NbTi superconductor is required, as close to superconducting as possible, there are a number of methods employable as the practice is commonly performed in large solenoids used in medical devices and NMR spectroscopy. [127, 128]. A summary of these ultra-low resistance techniques is found in 7.3.7

7.3.4 High Temperature Superconducting Tape

A high-temperature superconductor is one which has a T_c greater than the boiling point of nitrogen at 77K, allowing the much cheaper liquid nitrogen (LN_2) to be used as a wet refrigerant. LN_2 is also much easier to obtain, store, and transport, allowing superconductivity experiments to be performed without special equipment. A small dewar of LN_2 and simple expanded polystyrene container will suffice for many bench-top experiments.

For next generation planar magnetic sources, it is hoped to employ flat sheets of HTS to form unbroken HTS loops for persistent mode operation. The pieces are available in the form of YBCO tape from a number of manufacturers in standard thicknesses up to 12mm wide. We were able to acquire some samples of tape with a custom width of 40mm from *Bruker* and *American Superconductor*, though only short sections of a few metres in length were available as this width is not in current production. A sample is shown in figure 7.6. Persistent-mode YBCO tape operation is found in [19], so with some adaptations it should be possible to use this tape-based superconductor technology to create low-profile coil arrays operating in persistent-mode.

In addition to this, 2mm wide tape of similar formulation to the 40mm sample, was acquired from *Superpower Inc.* to handle the currents required for the prototype magnetic coils (8 wires in total), as the thick 0.8mm copper wire which would otherwise be required conducted too great a heat load for the cold head. Using 2mm HTS tape for this stage not only meant that cross sectional area could be reduced ($0.2mm^2$ compared to $0.5mm^2$, of which only $0.08mm^2$ is high-conductivity copper [129]) but crucially it meant that ohmic heating was completely eliminated along the length of the wire, and thus any length of tape could be inserted between the 1^{st} and 2^{nd} coldhead stages without any additional power dissipation. As heat conduction scales linearly with length, this allows the heat conduction to be reduced by simply using longer wires. Each segment

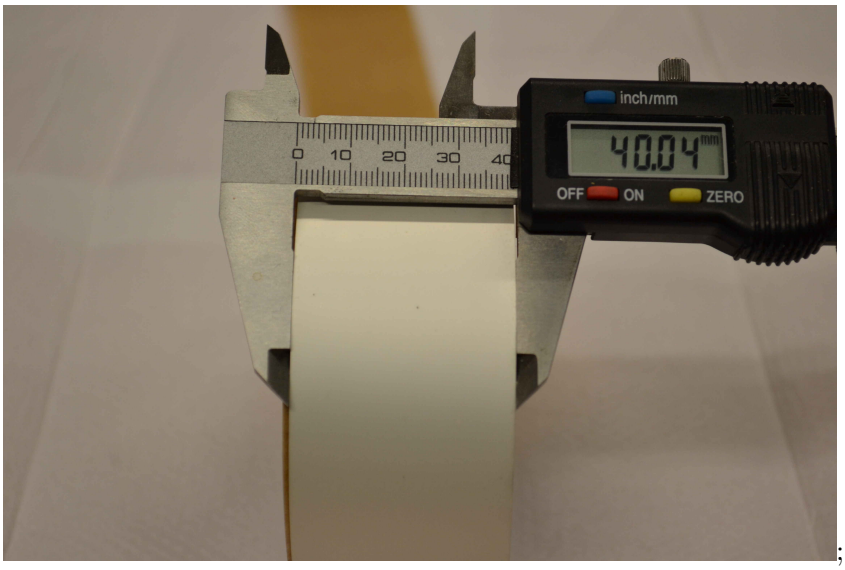

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FIGURE 7.6: A sample of the 40mm wide YBCO tape donated by *Bruker*. The tape is the same composition as the production tapes. For future versions of the planar magnetic field source, the tape will be engraved with the pattern of rectangular closed loops, to be operated in persistent mode [19].

of HTS wire is tested by the manufacture to establish a critical current (the production process results in varying I_c depending on cladding, stabilisers etc), and the specific sample acquired was rated at 40A per wire. This allows flexibility when compared to copper, as the current requirements of the coil can be changed, without re-optimising the wiring. The downsides of this HTS tape include that the bend radius is limited to 25mm, due to the nature of the YBCO ceramic, and the ribbon cross-section means that bending in a direction parallel to the flat surface is not possible without adding a twist or loop to the tape, and must be done with care. Soldering a low-loss joint is more difficult with the tape, (details below in section 7.3.5). Cost is also a downside, as the technology is still fairly new and thus expensive. As of writing this thesis the wire can cost around $30 per metre for 2mm tape, and up to $100 for the 12mm wide.

7.3.5 High Temperature Superconductor Joints

Joints between dissimilar conductors proved particularly challenging. That is to say, joints between the high-temperature superconducting tape used between the first and second cooling stages. This tape is comparatively fragile, as the superconducting layer is 1µm of brittle ceramic YBCO. This layer is encased within the structure of the tape [129]. If the YBCO is exposed in order to try and achieve a lossless joint - whether by chemical

or thermal processes - then the YBCO layer is at risk of losing its superconducting properties [89]. The ceramic itself does not solder with almost all common solders, and is damaged by heat over 150°C due to thermal loss of oxygen from the compound - breaking its superconductivity. Solders commonly used for difficult substances do not work well either, indium and indium alloy based solders will bond to YBCO, but will scavenge oxygen from the YBCO and form a barrier layer with poor conduction. This is also true for using a cold compressed indium contact.

All these points considered, it *is* still possible to join the tape with conventional solders, as soldering to the copper stabiliser is performed just like regular copper wire, with results in the nΩ range [130], provided that the temperatures are kept low and joint surface areas are kept high. While a nΩ joint is fine for current carrying applications, it is several orders of magnitude too high for persistent mode operation, as the industry standard requires joint resistances below the pΩ range [125, 131, 132]

7.3.6 Flux Pumping Method

Inducing persistent currents in a superconductor is not as simple as just invoking Faraday's law of induction, and superconductors have a number of properties which complicate the process. The law of 'Conservation of Flux' requires that any EMF generated in a coil by a changing magnetic field is subject to an equal and opposite EMF when the field is removed, thus no current is induced even if the conductor has no losses. It is necessary to employ a method known as 'flux pumping' to in effect 'smuggle' flux inside a superconducting loop, leading to a net gain in magnetic field. An example of this is shown in figure 7.8, results shown are taken during some preliminary evaluation of the process. In this test a closed loop YBCO tape was immersed in an open topped liquid nitrogen container, which allowed the CNC armature access from above, on which was mounted a small neodymium magnet. The magnet was then moved in a way which either dragged flux in (to increase the induced field) or out (to decrease) of the loop. A small amount of flux is trapped inside after each pass, gradually increasing the current in the loops, as shown in figure 7.7. While the preliminary testing was performed with a physically moving magnet to replicate techniques found in [133], with appropriate electronic timing systems and coils, this could be simulated without moving parts [20, 126, 134].

Flux pumping has been used with success in high temperature superconductor bulk to created permanent magnets [135].

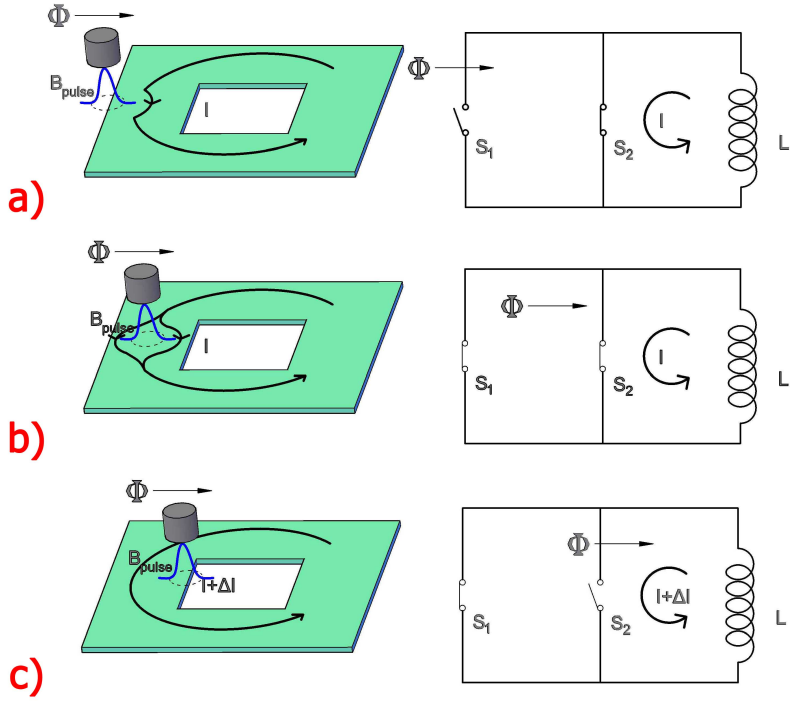

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FIGURE 7.7: A magnet is used to locally exceed the upper critical field of the superconductor on the outside of the loop. Flux can then penetrate the superconductor, and the region can be moved inside the conductive loop. When released, the flux remains in the loop [20].

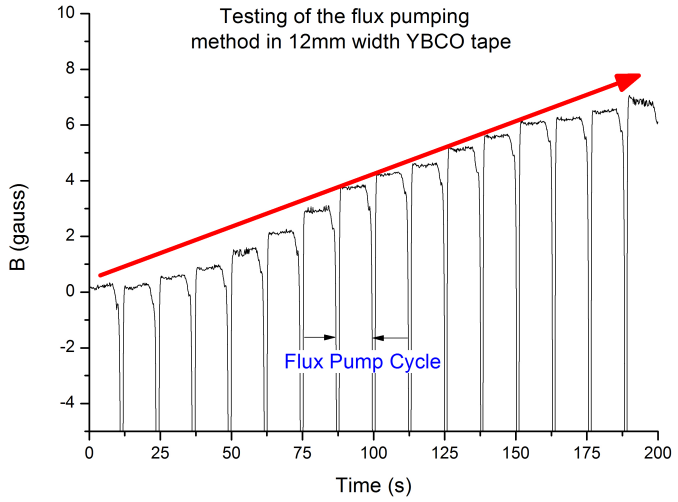

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FIGURE 7.8: Initial testing of the flux-pump method in YBCO. The test was performed by dragging flux into the centre of a loop of YBCO with a small neodymium permanent magnet mounted on an armature and controlled with the CNC machine. Between each 'pump' the field is observed for 10s.

Having numerous coils on the same axis and in close proximity to one-another presented us with the problem of cross-talk between each coil. As it is not possible to contain the magnetic fields such that no flux passes through the enclosed area of another loop, any change in flux will have an effect on the current flowing in any coils in close proximity. The effect is dependent on the distance between the coils and the strength of the magnetic fields involved, and will have to be taken into account when flux pumping close-proximity or concentric coils.

7.3.7 Low Ohmic-Loss Jointing Techniques

The low-loss joining of superconductors in our experiment was necessary for a two reasons. Firstly, when setting up a persistent mode current, unless there is absolutely zero loss in the system, there is an exponential decay of the current, which is a function of the resistance R and inductance L of the loop (equation 7.1) [125, 131].

In an ideal superconductor, the only source of ohmic resistance is the the joints between two superconductor sections. The second reason for minimising joint resistance is that any ohmic loss is converted directly into heat, which is of particular concern at the second (4K) stage of the cold head, which has just 500mW of cooling power. Local heating can be a problem, as if a localized area of superconductor is raised above its critical temperature T_c, then the superconductivity is broken and a runaway heating can occur, known as a 'quench', potentially causing damage to the system [136].

The key to a low ohmic joint is surface area. The larger the surface area of two joined conductors, the lower the contact resistance between them. Conventional solders can yield very good joint resistances, of a few nano-ohms, but due to variations in joint thickness and impurity inclusions, it is difficult to accurately predict the precise resistance of a joint. A large surface area is also key to good thermalisation, essential for ensuring all superconductors stay well below their critical temperatures, and any local heating is removed quickly and efficiently.

Chapter 8

Summary and Outlook

8.1 Summary

Starting from scratch, over the course of this PhD the current Geonium Chip project has been designed and built in its entirety. The challenges and solutions have been outlined in this thesis, and are summarised below:

- **Design of the Geonium Chip** The Geonium Chip was designed to fit the specifications outlined in [12], taking the specifications and translating into a form which could be made into functioning first generation chips. Details of the substrate, metallisation, via depth, electrode separation, wire capacitances and connection methods are all discussed.

- **Analysis of the Geonium Chip** The frequency response of the Geonium Chip and buried wires are measured and presented. From this the performance of the chip as a Penning trap can be estimated, and the loading on the detection system.

- **Computer Modelling** Simulations of essential processes such as the electron loading method, magnetic and electric field lower limits were explored through SIMION analysis, providing confirmation of the mathematical modelling carried out prior to this PhD, and provided industry-level tests of the ion paths within the trap.

- **Design of the Cryogenic On-Chip Vacuum Chamber** The directions taken in the design of the Cryogenic chamber are detailed. The chamber incorporates

a number space saving features, for example eliminating the requirement for any vacuum feedthroughs for signals, trapping voltages, and includes windowed optical access for the UV electron loading technique, while keeping the trapping volume electrically shielded. The UV loading removes the need for high-voltage/high heat electron sources, and can be completely DC shielded from the trapping volume. The photoelectric effect is also near instantaneous, and can be controlled by a simple switch, or intensity controller.

- **In-House Manufacture** The entirety of the cryogenic chamber and associated housing, mechanical fastenings were designed and built, and this process is detailed. The electroplating set up and plating results are discussed with the successes and failures of the gold plating on aluminium procedure. Having a rapid prototype system also capable of manufacturing experimental grade parts is extremely useful, and means that the experiment can be modified at any point, quickly and inexpensively.

- **Through-Chip Microwave Capabilities** The transmissivity of the chip is discussed, enabling near-field devices to couple to the electron at the cyclotron frequencies directly. This will serve in the future to provide a method of observing the cyclotron mode without any modifications to the chip design, instead allowing different devices to be put in close proximity with the trapped electron by simply placing within coupling distance of the electron. Though the cycltron detection is beyond the scope of this text, it is clear that this allows for a great deal of experimental flexibility.

- **Tunable Potential Landscape** The chip design includes additional electrodes which can be used to modify the potential in such a way that the electron motion is pushed in to ultra-elliptical regime, opening up new possibilities for direct cyclotron observation, and interesting new areas of Penning trap science.

- **Compact Magnetic Field** A pioneering compact magnetic field source is discussed, which represents an enormous reduction in both size and cost, as the magnetic coils generally required for Penning trapping and FTICR machines are by far the largest and most expensive component. Successful testing of the prototype will allow for optimization and improvements. The future optimisation steps are also detailed,

with an outline of the necessary steps to achieve the final goal of a micro-scale planar magnetic field source.

- **Detection Electronics** The detection electronics have been presented, as well as details on their performance characteristics. The in-house electronic manufacturing capabilities have been described, which afford greater flexibility in terms of board manufacture and the benefits of having a rapid prototyping system for electronics are discussed.

8.2 Outlook

The project is now extremely close to trapping its first electrons, a goal which is hoped to be realised in the very near future (*as of February 2016*).

While the Geonium Chip itself can trap any charged particle just the same as 3D Penning traps, the apparatus manufactured in this thesis is focussed on electron trapping and thus the first Geonium Chip experiment is fully dedicated to the goal of a 'quantum microwave sensor', a device capable of single-photon microwave detection in a multi-level system, as well as coherent quantum interactions with other microwave frequency devices.

In the future, the cryogenic chamber could be easily modified to allow injection of ions and charged molecules, using well documented processes currently used for FTICR cells and EBIT Penning trap mass spectrometers [37], and so could potentially be adapted as a compact mass analysis tool, with excellent accuracy to price ratio (a chart of where the Geonium Chip could fit into the mass spectrometry market can be seen in figure 1.1). Miniaturisation of the magnetic field and mounting directly to the chip will remove many of the field instabilities which many larger systems are subject to, for example nullifying the effect of vibrations, as the trap is physically attached to the magnetic field source. Persistent mode operation should offer excellent current stability, and will be largely impervious to external noise sources, particularly if the current is generated through a flux-pumping process. Thus with appropriate magnetic shielding, the magnetic stability can be made very stable indeed, opening up the possibility of the device being used for the fundamental measurements currently performed in 3D traps. The close-fitting cryogenic chamber detailed in chapter 5.2 has allowed the chip design to

be greatly simplified, stripped down to its most essential components. While this leads to a very compact system, it also means that in the next generations of the Geonium Chip, there are a great many possibilities when it comes to more advanced fabrication techniques, for example the use of superconducting layers makes feasible such modifications as in-substrate magnetic fields sources, in-substrate ultra high-Q resonators [137] e.g. for coherent cavity coupling, or even quantum devices such as Josephson junctions. Eventually, as the chip is built of the extremely well-known semiconductor substrate silicon, the cryogenic detection pre-amplifier system could even be incorporated into the chip itself, allowing for parasitic trap capacitances so low that the need for an inductive resonator is completely removed.

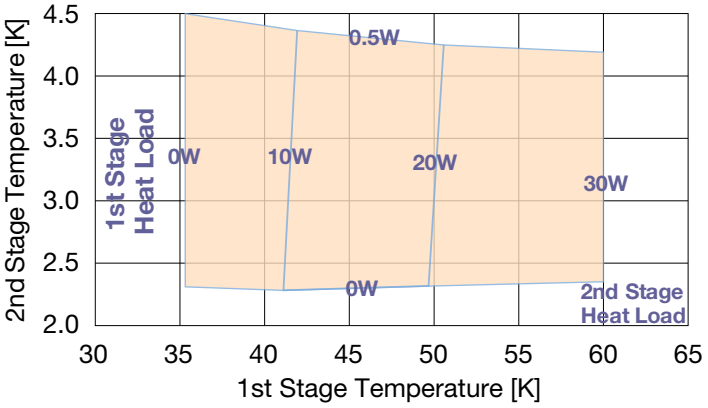
The Geonium Chip has many exciting prospects for the future, and represents a number of significant advancements in the field of compact and scalable Penning trap technology. With the advent of a working prototype here at Sussex, the Geonium Chip promises to deliver functionality with a wide range of applications, in both the competitive market and fundamental science areas.

Appendix A

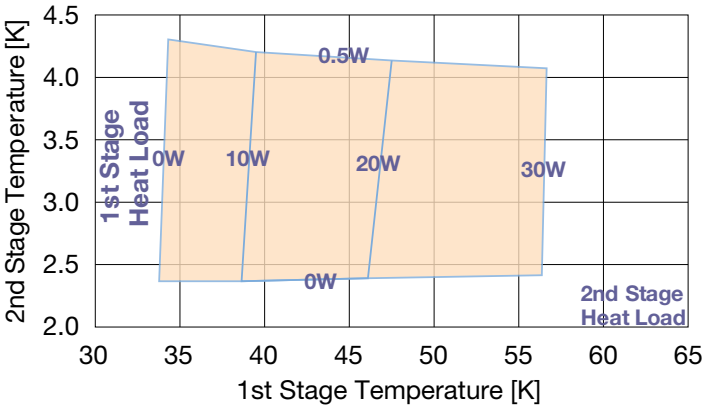
Appendix A

SHI Cryogenics Group

SRP-062B Pulse Tube Capacity Map (50 Hz)



SRP-062B Pulse Tube Capacity Map (60 Hz)



Note: Capacity maps for reference only. © SHI Cryogenics Group 3/12

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FIGURE A.1: Sumitomo capacity map of the *SRP-062B* pulse tube performance for various heat loads applied to the 1^{st} and 2^{nd} stages

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